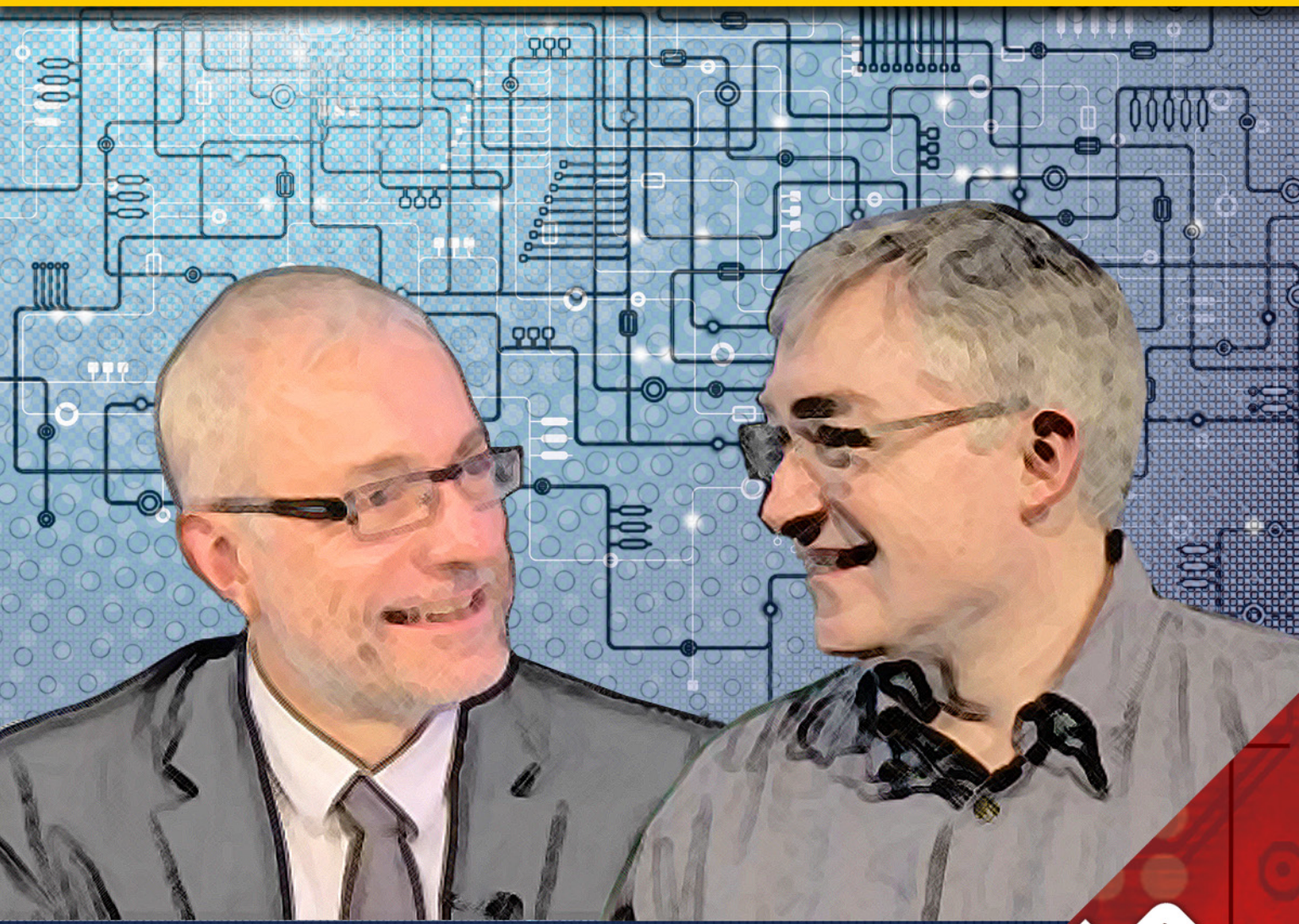
THE pcb design MAGAZINE

September 2014

AN I-CONNECT007 PUBLICATION

DATA FORMATS



The Great Gerber vs. ODB++ Debate

page 12

thepcblist

THE best way to find a PCB fabricator, anywhere.

SMG - Global Circuits, Inc.

Washington, Pennsylvania, U.S.A.

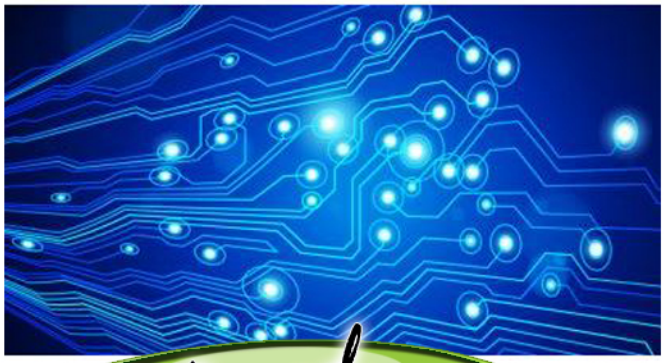
Website | Contact Me | RFQ

SMG Global Circuits, Inc. ISO 9001 CERTIFIED

Overview | Contact | Specs | About | Videos | Photos | Brochures | News

Our high-level performance as a printed circuit board manufacturer shows in our quality, delivery and service. It is this commitment to our customers that has earned SMG-Global Circuits an excellent reputation for providing printed circuit board manufacturing products at the lowest total cost of ownership in the industry, and satisfying a customer's most demanding needs.

Markets:	Communication, Consumer, Industrial, Medical
Board Types:	Single-sided, Double-sided, Multilayer
Mfg Volumes:	Prototype, Small, Medium, Large
Other Services:	Quick turn-around, Other: Domestic and Offshore Sourcing
Certifications:	IPC-6012 class 3, ISO 9001, ITAR registered, UL



Featured Showcase

Click here to see a demo

Click to see a partial list of registered OEMs!

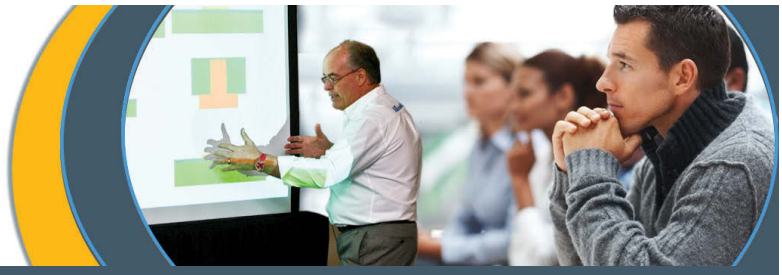
Why YOU should Showcase:

- Capabilities listing for advanced search functionality
- Specialties and certifications listing
- Ability to upload brochures and videos
- Quick and easy “Contact” and “RFQ” buttons
- News, web and contact links

www.thepcblist.com

Association Connecting Electronics Industries

IPC



Upcoming Events

September 23–25

electronica & productronica India 2014
IPC India Conference & Workshops
Bangalore, India

September 28–October 2

IPC Fall Standards Development Committee Meetings
Co-located with SMTA International
Rosemont, IL, USA

October 14–15

IPC Europe High Reliability Forum
Düsseldorf, Germany

October 28–30

IPC TechSummit™
Reliability. Innovation. Leadership.
Sponsored by: CALCE and Lockheed Martin
Raleigh, NC, USA

November 18–20

High-Reliability Cleaning and Conformal Coating Conference
Sponsored by IPC and SMTA
Schaumburg, IL, USA

November 20

Assembly & Reliability Conference
Bangkok, Thailand

December 3–5

International Printed Circuit and APEX South China Fair
(HKPCA and IPC Show)
Shenzhen, China

February 24–26, 2015

IPC APEX EXPO®
Conference & Exhibition 2015
San Diego, CA, USA

More Information
www.ipc.org/events

Questions?
Contact IPC registration staff at registration@ipc.org or +1 847-597-2861.

THE pcb design MAGAZINE™
September 2014

This Issue: DATA FORMATS

FEATURED CONTENT

The great data transfer format debate continues. This issue features an ODB++ update by Julian Coates, and the latest information on IPC-2581 by Hemant Shah and Amit Bahl. Plus, Coates and Karel Tavernier engage in a candid back-and-forth discussion about ODB++ vs. Gerber.

isola

Low-loss Laminate Materials for RF/Microwave/Millimeter-wave Designs

For over 100 years, Isola has been driving technology forward while improving end-product design with top-performing laminate and prepregs.

Our legacy continues with global R&D pushing our product line to the forefront in demanding RF/microwave designs.

With 10 manufacturing sites around the world, global quick-turn capability, world-class technical service, measurement & modeling capabilities, and industry leading material development capabilities – Isola is well positioned to be your preferred RF/microwave partner.

The newest members of Isola's growing RF/Microwave laminate family now includes Terra Green™, a halogen-free, very low-loss, thermoset material that is available in a variety of laminate and prepreg offerings. This material is inexpensive to process – improving your company's bottom line, as well as the environment.

Astra®MT is a revolutionary ultra low-loss thermoset laminate replacement for PTFE, suitable for automotive radar, mm-wave and AESA applications.

I-Tera MT is available in core thicknesses from 0.002" to 0.018" and offers 18 different prepregs for optimal design flexibility.

I-Tera®MT RF is available in 20 and 30 mil cores and a 3.38 and 3.45 Dk.

	TerraGreen™	Astra® MT	I-Tera® MT/ I-Tera MT RF	IS680
Tg	200°C	200°C	200°C	200°C
Td	390°C	360°C	360°C	360°C
DK @ 10 GHz	3.45	3.00	3.45	2.80 - 3.45
Df @ 10 GHz	0.0030	0.0017	0.0031	0.0028 - 0.0036
CTE Z-axis (50 to 260°C)	2.90%	2.90%	2.80%	2.90%
T-260 & T-288	>60	>60	>60	>60
Halogen free	Yes	No	No	No
VLP-2 (2 micron Rz copper)	Standard	Standard	Available	Available
Stable Dk and Df over the temperature range	-55°C to +125°C	-40°C to +140°C	-55°C to +125°C	-55°C to +125°C
Optimized Global constructions for Pb-Free Assembly	Yes	Yes	Yes	Yes
Compatible with other Isola products for hybrid designs	Yes	Yes	Yes	For use in double-sided applications
Low PIM < -155 dBc	Yes	Yes	Yes	Yes

NOTE: Dk Df is at one resin %. The data, while believed to be accurate and based on analytical methods considered to be reliable, is for information purposes only. Any sales of these products will be governed by the terms and conditions of the agreement under which they are sold.

FREE WEBINAR

PCB Material Selection for RF/Microwave/Millimeter-wave Design

This webinar will educate you on how to select the appropriate PCB material for RF, microwave and millimeter-wave applications through careful consideration of cost constraints and system-performance parameters, such as the frequency of operation and bandwidth, the electrical size of board and its critical features, loss and uniformity requirements, temperature range of system operation, and thermal and processing considerations.

www.isola-group.com/RF

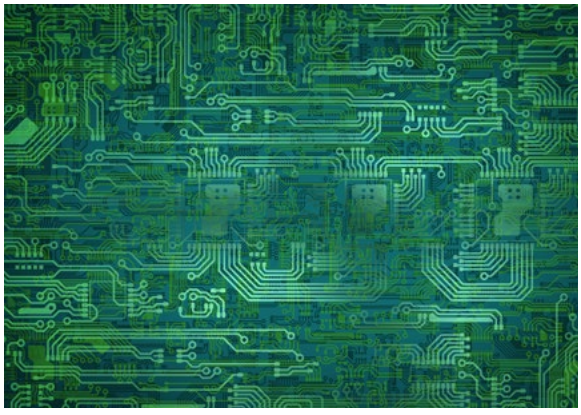
SEPTEMBER 2014
VOLUME 3
NUMBER 9
thepcbdesignmagazine.com

THE pcb design MAGAZINE™

THE OPTIMUM MAGAZINE DEDICATED TO PCB DESIGN

AN I·CONNECT007 PUBLICATION

CONTENTS

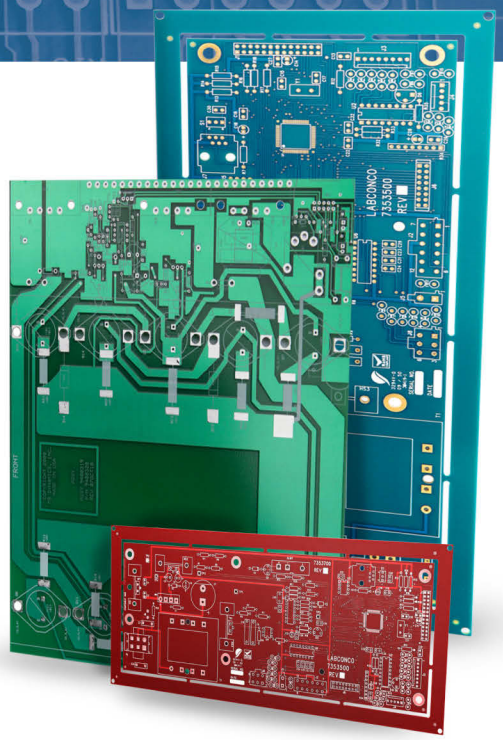


Quality PCBs from the established industry leader

With over 40 years of experience delivering high quality PCB prototypes, Sunstone Circuits® is committed to improving the prototyping process for the design engineer from quote to delivery.

We lead the industry with an on-time delivery rate of over 99%. Plus, our on-site technical support is available every day of the year (24/7/365), giving Sunstone unparalleled customer service.

Get a quote instantly at Sunstone.com



- Live customer support 24/7/365
- Over 99% on-time delivery
- Best overall quality & value in industry
- In business for over 40 years
- Online quote & order
- Free 25-point design review
- RF / exotic materials
- Flex / Rigid-Flex boards
- RoHS compliant finishes
- Free shipping & no NREs
- PCB123® design software
- Controlled impedance testing

SUNSTONE® CIRCUITS

40 YEARS SUNSTONE
40 Years of Serving You

Questions? Sunstone Technical Support is always open: 1-800-228-8198 - support@sunstone.com

The Survey Said: A Third of Designers Near Retirement Age

by Andy Shaughnessy
I-CONNECT007

One of the best parts of this job is keeping in touch with PCB designers. You all are an interesting bunch of people, to say the least, and I enjoy hearing your stories, concerns, complaints, observations about the industry, and whatever else you want to share.

I meet with some of you in person at trade shows during the year. But in between shows, a quick survey is a great way to get a snapshot of what you all are going through at the moment.

In July, we sent subscribers a three-question survey. We've noticed that surveys with too many questions often go unanswered. You're too busy to fill out a 50-question survey at work, so you forward it to your home e-mail address to look at later. Then you get distracted, rightfully so, by spouses, kids and grandkids. You just don't have much free time.

But you seem to have time to answer three questions. We had a solid response rate, especially considering it was the middle of summer. The replies are all over the place, particularly when we asked about technology.

Question 1: What is your approximate age?

I more or less expected this sort of age distribution, but it's still jarring to see it graphically. As you can see from Figure 1, over half of the respondents are 51 and over, and 1/3 of readers are 56 and over. The single biggest chunk of designers is 61 and over. Not a good thing for the future. How can we draw more young people into this industry?

Question 2: What are some of the challenging technologies you work with on a daily basis? (e.g., HDI, DDR3, differential signaling, high layer-count, etc.)

Here is a short sampling of the more common answers, slightly edited for clarity:

- High-frequency PCB design.
- RF, DDR3.
- The shrinking size of components!
- Diff pairs.

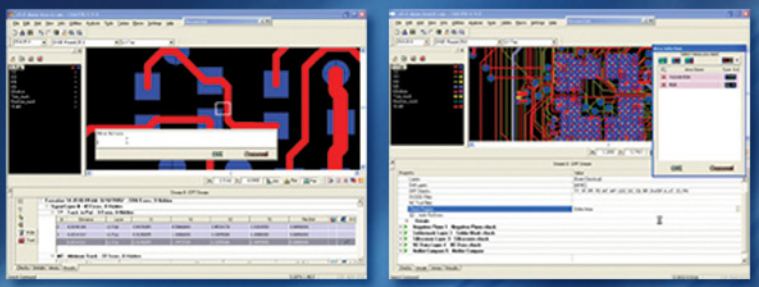
		Response Percent
1	21-25	2.33%
2	26-30	4.28%
3	31-35	7.00%
4	36-40	8.17%
5	41-45	12.06%
6	46-50	12.45%
7	51-55	19.07%
8	56-60	15.18%
9	61+	19.46%

Figure 1: The "age pyramid" for PCB designers. Who will design boards in the future?

Solutions to Ensure PCB Manufacturing Success!

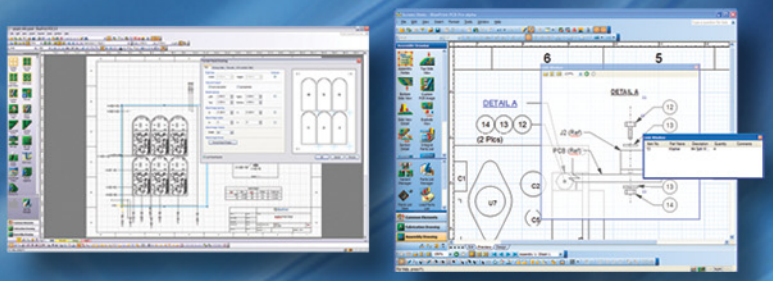
CAM350®

Verify and Optimize PCB Designs for Successful Manufacturing.



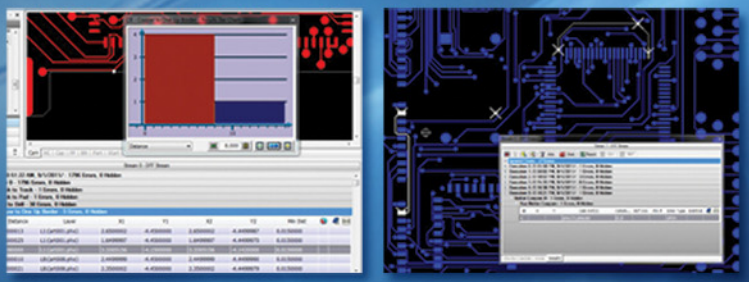
BluePrint·PCB

Create comprehensive documentation to drive PCB fabrication, assembly and inspection.



DFMStream™

Verify Design and Manufacturing Rules Any Time During the PCB Design Cycle.



At DownStream Technologies we are committed to delivering comprehensive solutions and workflow process improvements for all your PCB post processing needs.

For more information please visit downstreamtech.com or call 800-535-3226.

DownStream Technologies

THE SURVEY SAID: A THIRD OF DESIGNERS NEAR RETIREMENT AGE *continues*

• DDR2, SERDES differential signaling.

• High-voltage isolation, DDR3, SERDES length matching, low-noise design, power/ground and PDN design.

• The majority of the PCBs I deal with are very plain 2-layer boards. My specialty is not in high complexity, but how to provide beautiful boards at a price so low ordering becomes something you don't think about. Most of my repeat customers don't bother asking for quotes any more. I guess the most demanding "technology" for me is not actually technology, but language. The fabs I source from don't speak English, so it really puts my Chinese language skills to the test.

• Fine-pitch BGA, HDI, filled via-in-pad, high temperature (175°C), thermal management.

• HDMI DDR3 differential signaling, high signaling (14G) 16 to 20 layers.

• 100Gbps channels, embedded actives.

• HDI, DDRx, extreme copper weight, RF, thermal dissipation, .3mm-.4mm parts, ultra-low-noise circuits, 60-100 amp switching power supplies, planar core transformers, inductors, EMI-EMP, rigid and flex, medical and aerospace.

• HDI, high speed, lack of industry knowledge of customers.

• The challenges here all have to do with high power. So, voltage clearance, high current, heat issues, etc.

• High layer count. The challenges here are all to do with high power. So voltage clearance, high current, heat issues, etc.

• DDR4, rigid-flex, FPGA-PCB pin swapping.

Question 3. What is the best part of your job? Whether it's the design process itself, your great co-workers, your upcoming retirement, or something else, let us know!

• Generating end-products for use in space applications.

• The design process. As a service bureau, every job is different, with its own unique problems to resolve.

• The beach house it pays for.

• Working with a great bunch of people.

• Being paid to do puzzles all day.

• Learning new stuff.

• Our working environment would be the main reason that I still do this kind of work. Also, PCB layout designing is like playing Tetris all day!

• Parts placement is actually a fun puzzle.

• Working on new technologies for a great company, with occasional travel.

• Upcoming retirement in less than 18 months.

• With exception of our manager, no one is an expert in everything and everyone seems to chip in their part, which makes it all come together.

• The design process itself, plus great co-workers.

• The best part is working on international projects and creating sophisticated layout with high-end tools.

• Made a living doing this since for the last 36 years and enjoy doing it. Moonlight on the side doing it for former contacts. However, I do look forward to retirement down the road.

• Having the knowledge, gained by years of experience, to look at design proposal and see several ways it could be done. Being allowed the opportunity to build "designer confidence" by attending trade shows, reading tech articles and networking in turn allows me to build the confidence of a design team in my abilities is the best part of my job.

• I have a lot to learn yet!

• Sitting by a window and drinking coffee.

There you have it. You all love your work, and you enjoy collaborating with your co-workers. And I bet most of you enjoy sitting by a window and drinking coffee as much as that witty respondent.

But we're in danger of losing a big group of designers over the next decade or so. What can we do about the graying of our industry?

This column appeared in the Inside Design Newsletter *in August.* **PCBDESIGN**

Andy Shaughnessy is managing editor of *The PCB Design Magazine.* He has been covering PCB design for 15 years. He can be reached by clicking here.

Privately Held Global Printed Circuit Board Fabrication

LOCAL SUPPORT

and a *WORLD* of Circuit Board Manufacturing Options

USA GERMANY JORDAN TAIWAN CHINA

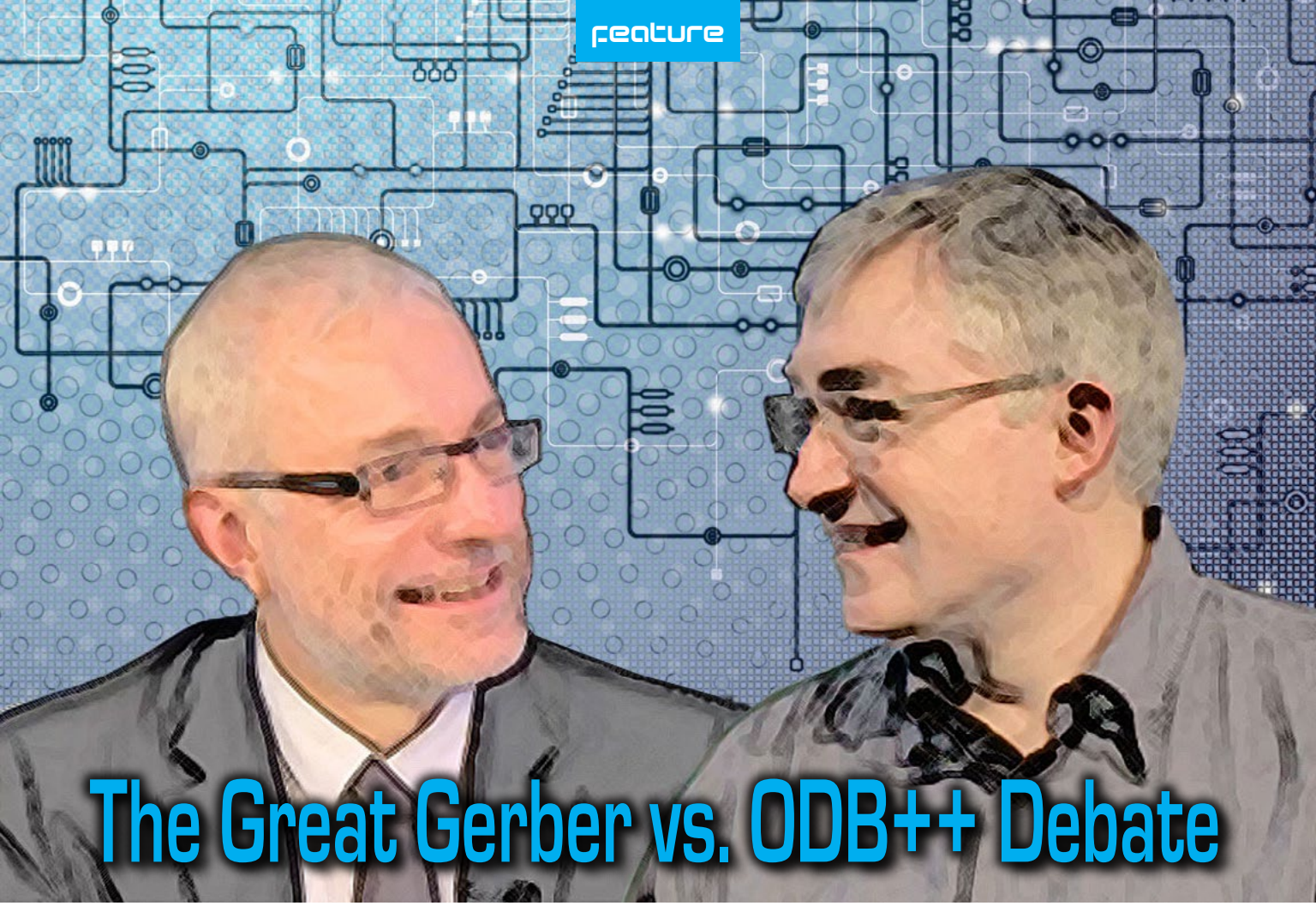
Manufacturing at ANY Volume, both On and Offshore
Quick Turn, Prototypes, DFM, Global Management
Specialties like Rogers, Aluminum, Hybrid Materials
Logistics including Consignment, VMI, JIT & More
24-7 Local Engineering, Service, and Support

Download Digital Brochure

Download Our Capabilities

HT
GLOBAL CIRCUITS

sales@htglobalcircuits.com | (727) 327-6236 | www.htglobalcircuits.com



The Great Gerber vs. ODB++ Debate

Editor's Note: This friendly debate (mostly friendly!) began with an article by Mentor Graphics' Julian Coates, which ran in the February issue of The PCB Magazine. *Karel Tavernier, managing director of Ucamco, which owns the Gerber format, replied to that article, and Coates was given the courtesy of a rebuttal so that they could be published side-by-side in the same issue. Finally, Tavernier replied to Coates, getting the last word...for now, at least.*

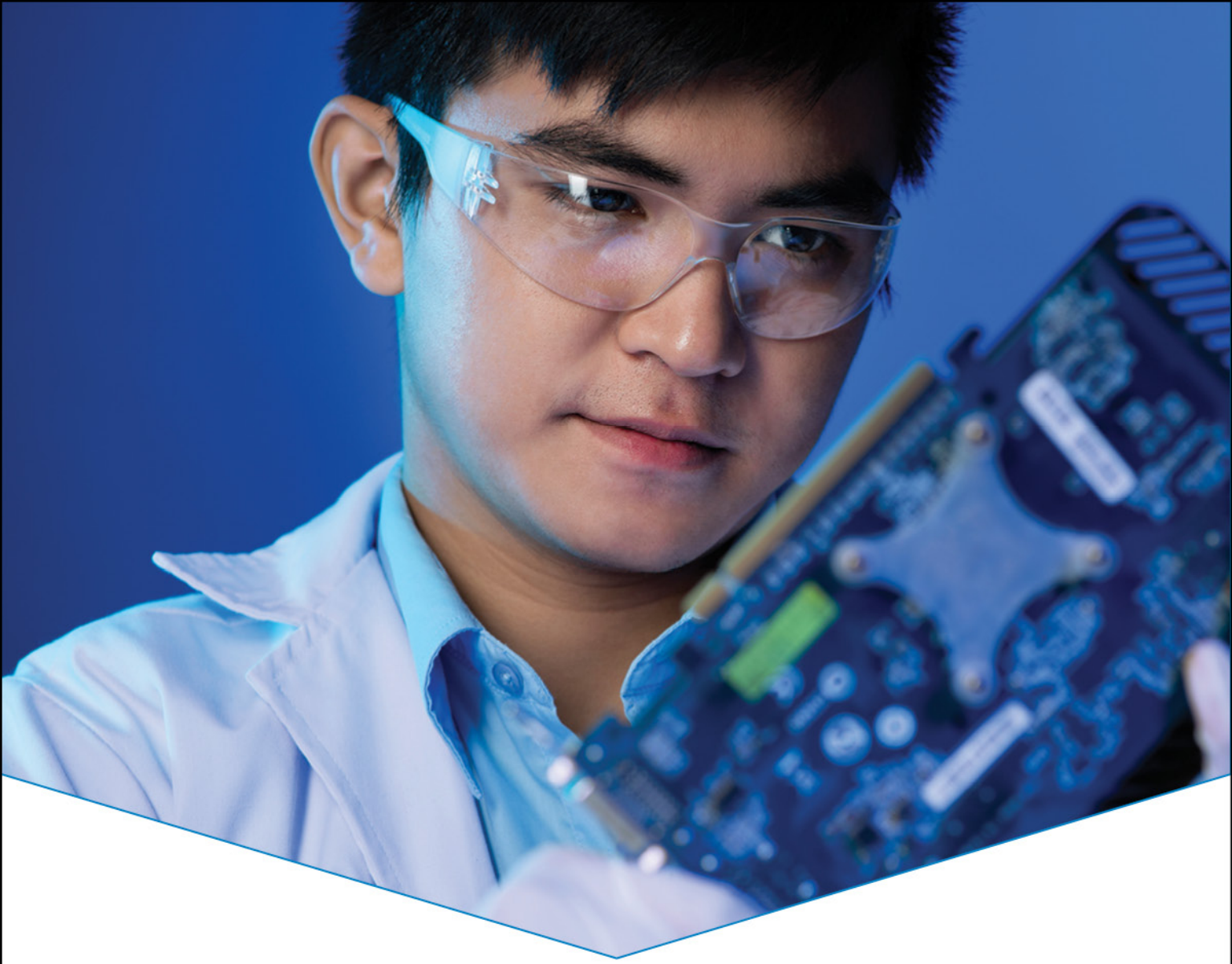
Gerber—the Smartest Way Forward

by Karel Tavernier

In a February 2014 article by Julian Coates of Mentor Graphics, Smart Data Formats Automate CAD/CAM, in which Coates promotes more widespread adoption of the ODB++ format, the arguments he uses indeed make it seem like OBD++ is the great panacea for our industry, one that promises to eliminate all problems for CAD-to-CAM data transfer without any downsides.

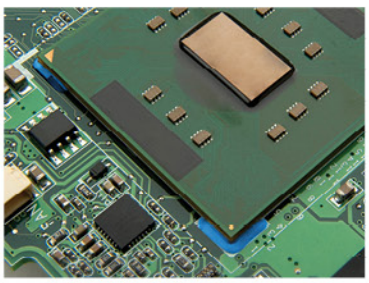
In order to promote ODB++, Coates unfortunately reverts to Gerber-bashing rather than explaining the strengths of ODB++. And his arguments are highly misleading, as they are based on some tired old fallacies that I would like to address here. Before starting, though, it's important to clarify that when referring to Gerber, I mean RS-274X Extended Gerber, the current Gerber format. This supersedes the earlier RS-274-D Standard Gerber format, which is obsolete. Bashing RS-274-D Standard Gerber is like railing against Windows because MS-DOS only allowed eight-character file names. If Coates wants to bash RS-274-D, I'll gladly join him. Having said this, less than 2% of all jobs are transferred using the old format, so it's practically a non-issue.

Extended Gerber is the PCB industry's de facto image data transmission format. New formats have come and gone; some, like the ODB++ format, have been around for decades, but still today, more than 90% of the world's PCBs, from



IT'S HIGH-PERFORMANCE RUGGEDIZATION. ONLY WITH MUCH HIGHER EFFICIENCY.

Dymax 9309-SC is the only light-curable edgebond material with patented See-Cure technology, giving you the speed and efficiency of visual cure validation with outstanding shock and impact resistance. And by holding its shape, 9309-SC minimizes capillary action and prevents material leaks. All this, backed by the Dymax Edge...an integrated offering of oligomers, customized adhesives and coatings, cure and dispense equipment, and application expertise to deliver the best solution possible. Visit **www.dymax.com/ruggedize** to request a product sample.



DYMAX.COM

DYMAX®

877-396-2988

the simplest to the most complex, are still manufactured using Gerber, which tells me that this is an image format that the industry trusts. And the industry is right to trust it—it's the best there is. Used properly, it delivers on its promises, without fail, every time.

So let's have a look at some of Coates' arguments. He quotes Viasystems as stating that, "about 25% of the data packages they receive have issues relating to:

- Missing layers, fabrication drawings, drill files, etc…
- Netlist format violations
- Netlist exception violations."

If true, this is indeed a sorry state of affairs, and needs rectifying. But if this is the extent of the problems, then there is nothing wrong with the format. Viasystems' issues are in fact due to some rather trivial bugs in the CAD vendors' implementations, so the solution is to fix the implementations rather than to adopt completely new software by switching to a new format. The article is not clear about whether these omissions and violations relate to ODB++ or Gerber files, or a mix of the two. However they arise, I can only recommend that Viasystems report these issues to their customers with a request to contact their CAD software suppliers. If the CAD software vendors fix these simple bugs, the issues will be resolved once and for all. If they are unable or unwilling to do so, there is no solution: neither in Gerber, nor in ODB++, nor anywhere else for that matter.

Coates also mentions that Gerber files sometimes contain syntax errors, low numerical accuracy and other errors. This is no doubt true, but again these are simply bugs in the Gerber output. Do we need a new format to fix syntax errors in the current one? Surely the solution is to fix the bugs in the Gerber output. And ODB++ itself is not immune to syntax errors; if anyone would like some invalid ODB++ files, I can provide a few.

The reality is that Gerber files very rarely generate the wrong image. This is because while only a few applications read ODB++ reliably, there are countless more that read Gerber with near-perfect reliability. This is because:

- The Gerber format is simple
- Its specification is well-written, easy to read, detailed and precise
- Most of its implementations are mature
- As it is so widely used, the implementations are thoroughly field tested, so most bugs have been ironed out
- The format is supported by excellent free viewers such as GC-Prevue

Advocating the adoption of a new and much more complex format to eliminate simple bugs is a very curious solution indeed. Consider only that a CAD software developer struggling to produce a simple Gerber file correctly is not miraculously going to write a bug-free implementation for the more challenging ODB++ format. If one wants bug-free software it is best to stick with Gerber, as Gerber is a simpler and more mature format than ODB++, it is far less prone to bugs, and its bugs are far easier to find and resolve. Switching to a new imaging format introduces a whole raft of new issues and bugs that would take many years to sort out. Imaging software is complex and takes a long time to get right. Adopting ODB++ to solve bugs in Gerber output is like using a sledgehammer to swat a fly: The solution is far more damaging than the issue ever will be.

Table 1 summarizes Coates' claims regarding the benefits of ODB++ vs. Gerber.

Here is my take on the aforementioned benefits:

1. False. A simpler, more reliable format in fact needs less diagnostics
2. False. An error can be more easily identified in a simpler format.
3. False. ODB++ is not miraculously error-free.
4. False. IPC-356 supports the actual customer net name. It may be that the software Coates uses does not display it, but this then is a problem in that software.
5. False. Gerber has negative apertures and so can handle planes perfectly. (I should add that this is the first time I see the claim that ODB++ is more compact than Gerber!)

If these are the benefits of ODB++ and the reasons for adopting it, then Coates' argument collapses.

More importantly, Coates omits to mention the difficulties in adopting ODB++. Over the 20 years that ODB++ has been available, it has taken just 10% of the market share, with Gerber accounting for the remaining 90%. If ODB++ offers all the advantages espoused by Coates in his article, there can only be one of two reasons for its minimal uptake:

- The PCB industry consists largely of morons
- There are downsides to using ODB++

As I do not think this great industry is in the hands of morons, I believe that there must be some serious downsides to the adoption of ODB++. This is not because ODB++ is a particularly bad format: It is not. The point is that the adoption of ODB++ includes the adoption of a new image format, and image formats are notoriously hard to implement. Much has been written about just how complicated geometric software is and how much effort it takes to get it right, not to mention the years it takes to debug. So the implication that taking on this new image format is simple and low risk is at the very least misleading. Precisely because our industry's practitioners are not morons, they know this, so are reluctant to adopt a new format. They know very well how complex ODB++ is, and that it will give rise to many more problems, for many years.

The reality is that Gerber works very well for transferring images. In fact, there's nothing better.

Gerber X2

The most interesting point made by Coates is that Gerber files contain "no information about how the PCB layers stack up." This was a valid objection in the past, but it is no longer true, as the latest revision, Gerber X2, now contains layer stackup information.

At the heart of X2 is the use of attributes. These are akin to labels which provide information that are associated with image files, or features within them. The beauty of using attributes is that they are already familiar to CAM professionals and software developers, and they

sit naturally with the current capabilities of CAD and CAM systems. X2 extends the current Gerber specifiation with a series of standard attributes that are most important for efficient CAD-to-CAM communications, such as the function of each layer, whether a pad is a via or an SMD pad, and which are the component drill holes. As rather grandly stated elsewhere, X2 adds intelligence to the Gerber format. Software supporting X2 will read the whole Gerber archive automatically, with all layers in place, while identifying the function of each object.

Easy to adopt and to implement, X2 is upwardly compatible with the previous Gerber version. Altium, global leader in Smart System Design Automation, has been quick to recognise the value of X2 and will support it in an upcoming version of Altium Designer. By Q4 2014, Graphicode's widely-used and highly-respected GC-Prevue viewer will also support X2.

X2 maintains the trademark simplicity for which Gerber has always been known and used, and gives designers and engineers a standardized procedure that will require very little to change in their working practices—certainly none that would require approval, testing and all the rest. Equally important, this new revision does not disrupt existing workflows. If the software does not support the new capabilities, the old workflow continues to operate. Nobody is forced to buy anything. So this will be a very gentle, low cost improvement indeed, but the effects will be nothing short of revolutionary.

Coates omitted to mention this latest development in the Gerber format, one of the most

important developments in CAD-to-CAM automation today, given that it concerns the industry's de-facto standard format. Neither did he mention the alternative IPC-2581. Had he done so, his arguments for ODB++ might have been less compelling of course, but these omissions in an article titled Smart Data Formats Automate CAD/CAM lead to serious doubts about its objectivity.

Coates also added a diagram to the article comparing Gerber to ODB++ input in CAM. This compared a badly implemented Gerber with a well implemented ODB++. I have taken the liberty of adding a proper X2 Gerber to the schematic. The result, given in Figure 1, shows that if ODB++ is a smart format, Gerber X2 is a very smart one.

Conclusion

When CAD-to-CAM data sets use properly implemented Gerber archives, plus correct IPC-356-A files, problems in data transfer are rare. Where a problem or bug appears, the easiest, fastest and most economical solution is to fix it. This is because issues are not down to the format itself, but more likely due to its implementation in CAD software, and they are simple to resolve. The very worst solution would be to replace Gerber with the far more complex ODB++ format, because implementing a new format is never simple, quick, and/or risk free, especially when the new format is as complex as ODB++. The problems that would arise from such a move would be significant, and would hound the industry for many years.

The simplest, most practical path forward is to fix bugs in current implementations, and adopt Gerber X2 functionality.

One of the best things about this path is that it is incredibly kind on the industry, while enabling the PCB industry to benefit from all the advantages that ODB++ claims to deliver in Coates' article, but with none of the downsides. This is because it does not involve the wholesale adoption of a new format. Furthermore, the revised Gerber format is compatible with the previous versions of Gerber and older software, so improvements can be as gradual as users want them to be, with no one being forced to buy new software against their business wishes or budgetary constraints. It is a path that delivers to small software vendors and the industry at large, fixing what is broken without compromising what already works. In short, it's nothing short of revolutionary, but without the complications.

The Gerber format specification, a sample X2 archive and background articles on X2 can be found at www.ucamco.com/downloads.

Karel Tavernier
Managing Director, Ucamco

Julian Coates' Rebuttal:

With respect to Karel, I think he may be missing the main point. Consider this:

- No doubt Gerber is a very fine format for defining the graphical layers of a PCB
- IPC-D-356 is perfectly fine for defining a netlist

ODB++ Benefits for the PCB Fabricator
1. Import and export diagnostics are significantly reduced compared to Gerber
2. Errors can be identified and communicated to the customer much earlier in the process
3. Eliminates format errors and net exceptions that are common with Gerber
4. Fabricator can be allowed to see actual net name used by customer, easing the process
5. Less data is required for handling positive planes

Table 1.

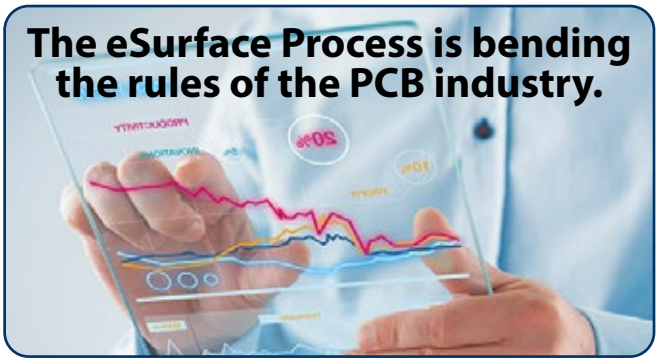
Designers, meet your new best friend.

Murrietta Circuits' partnership with eSurface gives you the very rare ability to increase circuit density while decreasing cost!

Every great board begins with a great design. With no substrate restrictions, designers can utilize new PCB materials with high performance attributes to their maximum potential. Not only does eSurface reduce costs and shorten production time, it meets or exceeds MIL/IPC specs!

"We truly believe that this technology will not only change the way that boards are manufactured, but change the way boards are designed."

Andrew Murrietta



Click to learn more

Murrietta Circuits
The Integrated Solution

www.murrietta.com | (714) 970-2430

- Excellon needs no improvement; it defines the location and diameter of drilled holes quite well.
- Component placement lists can define component positions and rotations quite well also
- PDF is a good format for rendering drawings
- GenCAD and FATF are good for defining the parts of a PCB assembly for testing purposes
- Word is good for capturing text, especially "Readme" documents that explain to a CAM engineer how all of the above file-types should relate to each other, and how to reintegrate all that data back together so as to enable an efficient software-driven new product introduction (NPI) process.

Certainly, if all you want is accurate graphical data, then I am sure Gerber meets the requirement, and Karel is to be congratulated on his perseverence in improving that particular 50-year-old NC format. At a recent industry debate on this topic, he suggested that the best

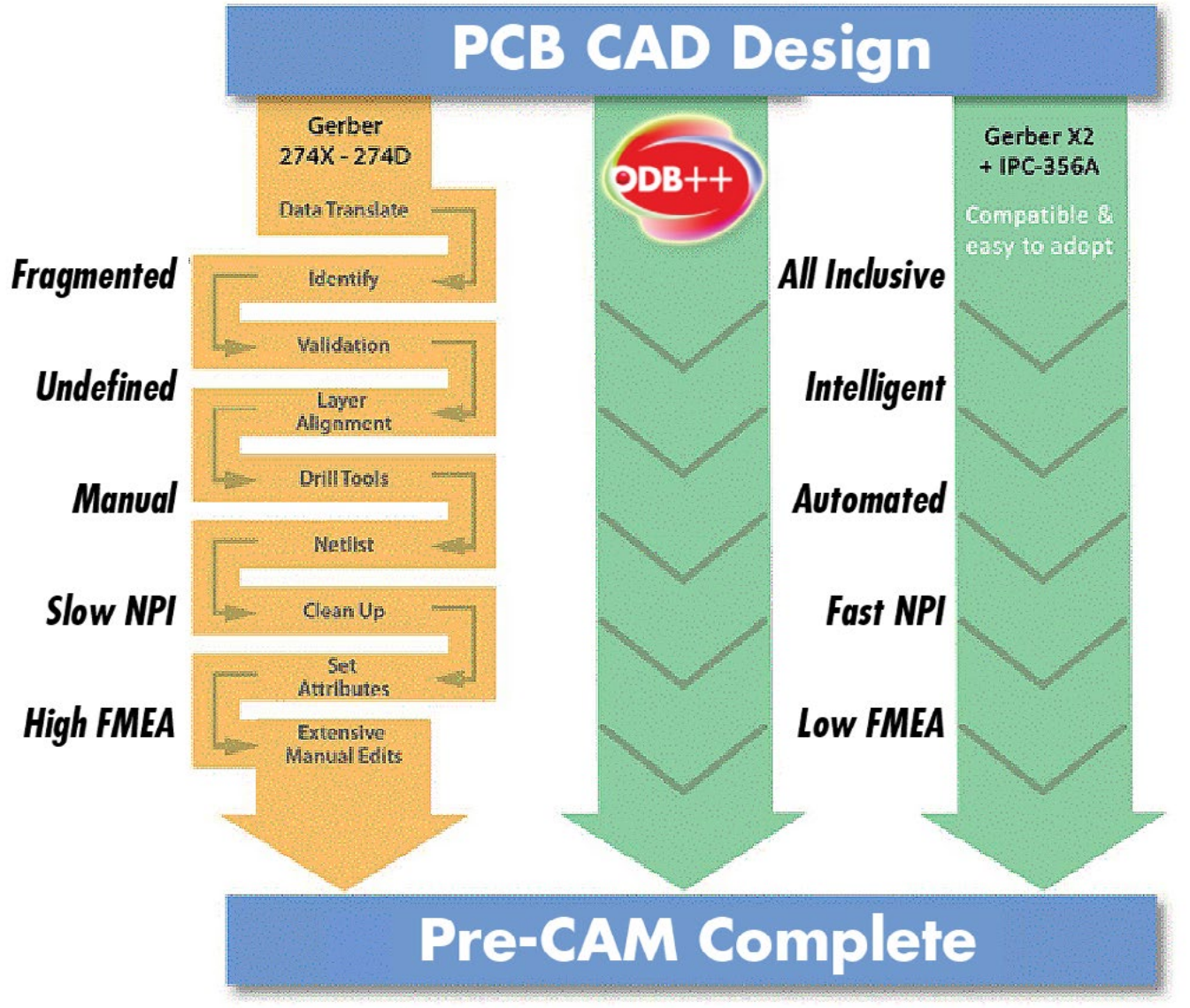


Figure 1: The column on the right can be achieved at low cost, without breaking workflows, in an upwardly compatible way.

way forward is to use Gerber for the graphical data and another format for all the other information that Gerber cannot carry. Thus, he promotes the idea of intelligent, all-encompassing formats for carrying data, but excluding the graphical part. Why reject the advantage of having all of that other information linked to the graphical objects as well, and vice-versa? The problem that needs solving is taking all of that fragemented data into a single coherent model comprising both the PCB bareboard and the assembled PCB. Keeping parts of the product-model seperate for simplicity is fine if you are only interested in a narrow subset of the PCB product-model, but it is a big problem if you need a complete definition of the product, as do all DFM and NPI engineers! There is no escape from the fact that, sooner rather than later, the data must be integrated.

Reductio ad absurdum: To take the idea to an extreme, maybe there is a drilling expert out there ready to explain that Excellon should be used for holes information, but all of the "other information" (including the layer graphics, no doubt) should be carried in ODB++. Obviously it is absurd to keep part of the PCB product-model (in this case, the holes) separate from all the rest. The first thing a CAM engineer would do in this case would be to read the Excellon file and integrate the hole data into the ODB++—an unecessarily time-wasting and potentially error-prone process.

There is a broad consensus across the industry that fixing the highly fragmented nature of the CAD-to-CAM data files problem is long overdue, and that the answer is to implement integrated, intelligent formats such as ODB++. Many have already taken the step with ODB++, attesting to the benefits of having a more streamlined design-to-manufacturing hand-off process. Over a million different PCB designs have been processed into manufacturing using the ODB++ format since its introduction. It works, and is widely implemented by some of the largest electronics OEMs in the world, as a standard part of their NPI business process.

What limits the implementation of ODB++ more widely? Why do people still use all those fragmented narrow-scope data formats such as Gerber, Excellon, netlist, component-placement list, etc? I would suggest that the reason is not technological; it is a combination of business and human factors. Firstly, it costs money to change a business process; tools have to be upgraded. But in order to gain the time/cost/quality advantages, an investment has to be made, and that is nothing out of the ordinary. Secondly, there is a perception that continuing to use the old method is not only free but also "safe," whereas to use the new method is expensive and "uncertain." The "safe" versus "uncertain" part is the human part. There is an jargon-acronym for it: FUD, which stands for Fear, Uncertainty and Doubt. The same was true when the Gerber format was introduced. Using it required a high level of investment, and it took time for the industry to see that the benefits outweighed the uncertainties even though the idea of it was obviously a good one 50 years ago. Hand-drawn artwork was still used for many years after, even though a better method (Gerber data) was available. It took time for the industry to make the change. But change is inevitable if businesses intend to advance given the complexities of today's systems designs. This is why I advocate ODB++ as the new data format standard.

Julian Coates
Director of Business Development
Valor Division of Mentor Graphics Corporation

Karel Tavernier's Rebuttal:

And the Data Transfer Beat Goes On...

In a recent article, Smart Data Formats Automate CAD/CAM (February 2014), Julian Coates of Mentor Graphics wrote an article about the ODB++ format. My reaction to this, Gerber—the Smartest Way Forward, appeared in the July 2014 edition of the same publication, as did a rebuttal by Coates of my article.

Here I would like to rebut Coates' rebuttal of my rebuttal. To be merciful on readers, I will keep it brief, so that the rebuttal process converges rather than spinning out of control.

In Coates' July rebuttal, he wrote: "No doubt Gerber is a very fine format for defining the graphical layers of a PCB."

That's good. My impression was that Coates saw Gerber as an intrinsically error-prone image format whereas I maintain there are very few errors when transferring images in Gerber. So we both agree that Gerber is a very fine image format. Where our opinions diverge is in how we proceed from this fact. Coates went on to state: "At a recent industry debate, I suggested that the best way forward is to use Gerber for the graphical data and another format for all the other information that Gerber cannot carry."

Thus, he promotes the idea of intelligent, all-encompassing formats for carrying data, but excluding the graphical part. Why reject the advantage of having all of that other information linked to the graphical objects as well, and vice-versa? The problem that needs solving is taking all of that fragmented data into a single coherent model comprising both the PCB bareboard and the assembled PCB.

Actually, in no way do I reject the idea of linking all the other information to the graphics objects. On the contrary: It's clear that a PCB is more than a set of images, and all the data describing it must be transferred as a coherent whole. Here, too, we agree. Where we disagree is how we achieve this coherent whole. Coates believes that the wholesale adoption of ODB++ is a practical way forward. I do not. In another passage from his July rebuttal, Coates correctly analyses why ODB++ is not more widely used:

"What limits the implementation of ODB++ more widely? … I would suggest that the reason is not technological; it is a combination of business and human factors. Firstly, it costs money to change a business process; tools have to be upgraded. […] Secondly, there is a perception that continuing to use the old method is not only free but also safe, whereas to use the new method is expensive and uncertain. The safe versus uncertain part is the human part."

These are entirely rational and justified concerns, and clearly the vast majority of this industry feels that they outweigh the benefits of ODB++ (or of any new format that has been tried over the decades for that matter). Who am I to judge that the whole industry is wrong? That said, our industry must move on, and like Coates, I too would like to see CAD to CAM data transfer advance beyond current practices. This is why I propose a path that is far less expensive and risky than that advocated by Coates.

The first step along this path was to clarify areas in the Gerber format specification that were sometimes misunderstood, and to remove elements in it that were outdated, rarely used, or superfluous. This has been carried out in recent years, so the current spec is clear, sharp and to the point—there are no useless bells and whistles in the Gerber format.

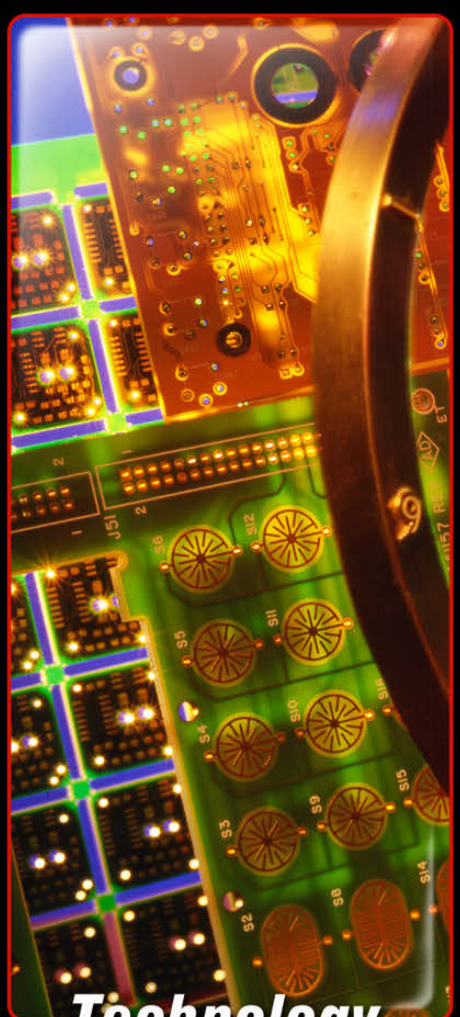
The second step, completed earlier this year, was to introduce the Second Extension, or Gerber X2 format. Gerber X2 contains attributes that specify how the layers stack up, identifies via pads, indicates where the impedance controlled tracks are, and describes a host of other parameters that support the image data. With X2, what was missing in Gerber has now been added—in Coates's terminology, the attributes add intelligence to the format. The neat thing is that they do not affect the image, which means that existing workflows are not broken: X2 requires only minimal changes in working practices, and certainly none that would require approval, testing and all the rest. The fully X2-compatible CAD and CAM software will read entire Gerber X2 archives automatically, with all layers in place, while identifying the function of each object. And even in combination with older software that does not support X2, the correct image is still produced. This means that even if users do not reap the full benefits of Gerber X2, they can happily move within the X2 world without problems. Ben Jordan of Altium concurs: "ODB++ is a good standard, but Gerber X2 does solve the problems while being backwardly compatible."

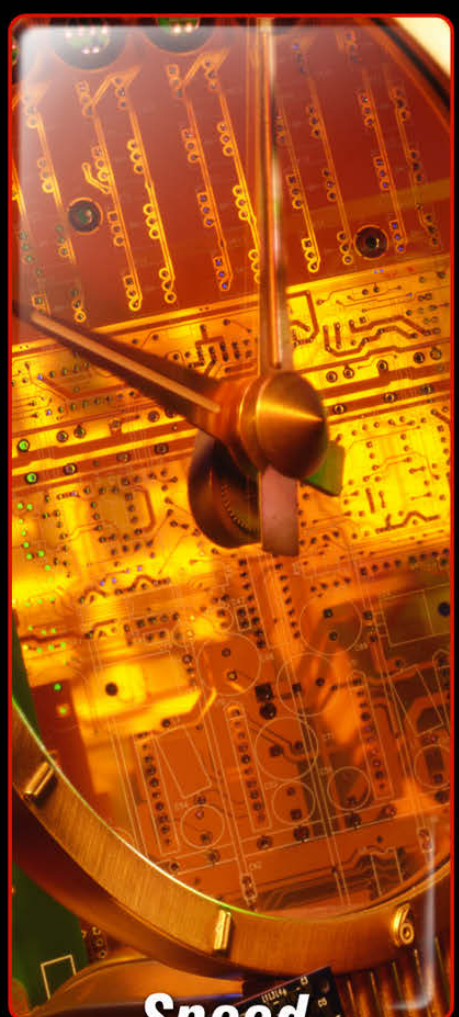
More importantly, this means that nobody is forced to buy anything, and Gerber users can decide in their own time if, how and when to adopt new X2-ready software to take their processes to the next level. For those interested, there is a sample X2 job on the Ucamco download page. It shows the simplicity of the concept. Download it and try it on your own Gerber input software—in all probability you will be able to read in the images correctly, but your software will throw some warnings. This demonstrates the compatibility of X2 with non-supporting software.

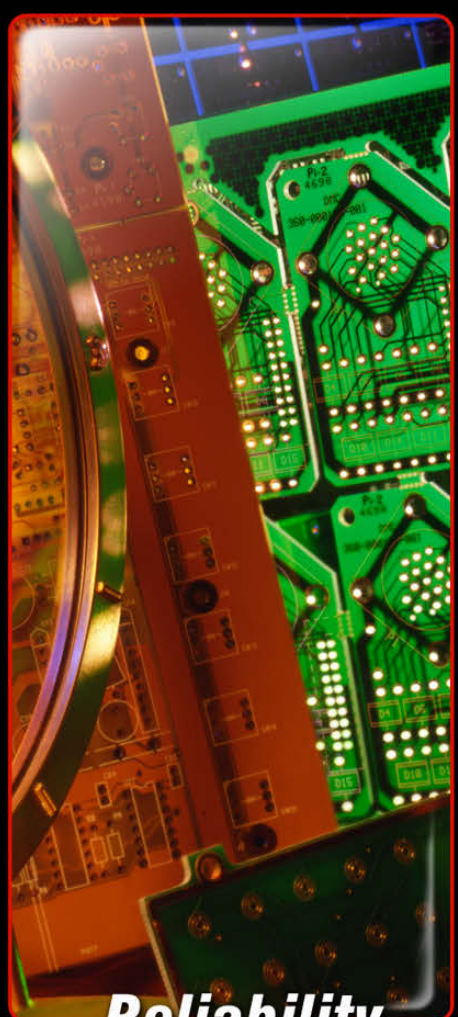
prototron.com

We Take the Time to do it Right

because you don't have the time to do it over.







Prototron Circuits

High quality quick turn manufacturing, just another reason we are

America's Board Shop

THE GREAT GERBER VS. ODB++ DEBATE *continues*

Coates makes much of the claim that ODB++ is a single format and that what I propose is a collection of different formats. This underpins his argument that the good old Gerber format should be dumped and replaced with something entirely new. This is a curious argument indeed: ODB++ is in reality a collection of folders with different syntaxes for each type of data, which are all zipped together in a single archive file. In my opinion this is not a showstopper—on the contrary, it's an inevitable consequence of the fact that components, materials, graphics and netlists are all entirely dissimilar objects. They must all be stored in appropriate formats, each of which, by its very nature, is very different from the others. All they have in common is the ODB++ name. This is clearly demonstrated by the following: if ODB++ image input is implemented in your software, it will not miraculously read materials. Even though you may be able to write images, you cannot automatically write a netlist. These are separate items that require individual implementation, each with its own specification, each in its own folder. This is OK; it is impossible to put these intrinsically different objects into the same format. But I fail to see the difference between zipping together a collection of very different ODB++ folders, and zipping together Gerber and IPC-D-356A files. To anyone who might object that 356 is a different format from the Gerber format, I would propose the following thought experiment: Take the 356A specification, tear off the title page and replace it with a page with the title "Gerber Netlist Format." Lo and behold, now, images and netlist are in the same Gerber format! In other words, there's no substance to the claim that ODB++ is a single format—it's all in the name. Of course, in both cases, the information must be consistent. If you offset the netlist to the image, well, you have a problem, both with Gerber and ODB++.

What I propose is that we, as an industry, take a practical and pragmatic route to improvement: by keeping what works well, changing what does not and adding what is lacking. With Gerber X2, we are doing just this, as Graphicode's Paul Wells-Edwards points out: "The beauty of Gerber is that it's simple, and very widely used, and Ucamco's use of attributes is a very clever and straightforward way to improve and build on it. By extending the format and making it far clearer, Ucamco has improved the CAM task no end."

Indeed, it makes no sense whatsoever to totally abandon something as good as Gerber's image format, which covers the most difficult and critical part of any PCB data archive, to resolve issues relating to the archive's far simpler elements. The industry intuitively senses this, and this is why it has stayed with the Gerber format.

X2 has been designed to be easy to implement and easy to adopt, as it consists of just three new straightforward commands, and support for it is growing. Graphicode is pioneering the X2 wave with GC Prevue v22.3, the industry's first X2-ready viewer software, which is now available for download. Altium too has been quick to recognise the value of X2 and will support it in the upcoming version of Altium Designer. I was recently informed that DipTrace and Kicad will also output X2 in the course of 2014, and LPKF will support it from Q1 2015. Eurocircuits and AT&S offered to beta test it, and it will be in real production by the end of 2014—less than 12 months after its introduction. This demonstrates the benefits of smart improvements: fixing what is broken but leaving in place what works well, which takes into account the community's legitimate concerns about cost and risk.

This is why I advocate X2 as the smart way forward.

Karel Tavernier
Ucamco

Thermal management solutions that perform when the heat is on

With a consumer requirement for ever-more diminutive devices and an expectation of improved efficiency and power, effective thermal management materials have become an increasingly essential part of product development.

From bonding and non-bonding thermal interface materials, to thermally conductive resins, our solutions offer the ultimate level of protection and heat dissipation.

With an expansive product range and a strong emphasis on research and collaboration, we provide a complete electro-chemical solution to the world's leading manufacturers across a variety of industries.

Isn't it time you discovered how Electrolube can serve you? Simply call, or visit our website.

Scan the code to discover our full spectrum of superior Thermal Management and electro-chemical solutions.

Tel: 888-501-9203

www.electrolube.com

ELECTROLUBE

THE SOLUTIONS PEOPLE

Electronic & General Purpose Cleaning	Conformal Coatings	Encapsulation Resins	Thermal Management Solutions	Contact Lubricants	Maintenance & Service Aids

IPC-2581 Adoption Update

by Hemant Shah and Ed Acheson
CADENCE DESIGN SYSTEMS

Intelligent, efficient PCB design data transfer to manufacturing has been a hot topic for the last three years. A small group of companies created the IPC-2581 Consortium in mid-2011. Since then, many companies joined the effort to get IPC-2581—an open, neutral, intelligent format—adopted. It has been a wonderful journey that witnessed unprecedented collaboration amongst PCB design and supply chain companies, innovation with stack-up exchange, and last but not least, steady progress toward adoption. This article provides an update on IPC-2581 Consortium activities that include collaboration, innovation and adoption status.

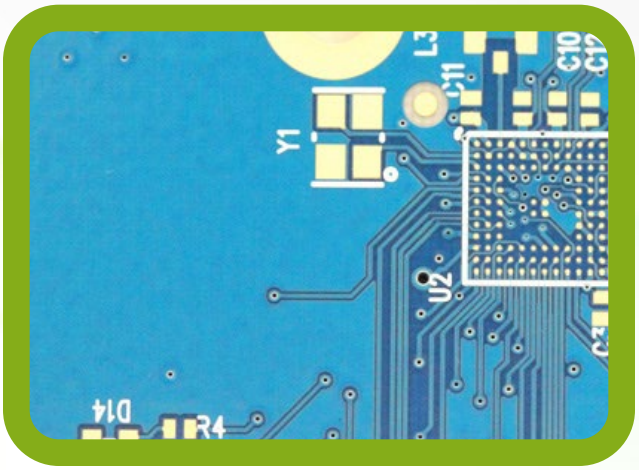
The IPC-2581 Consortium for an open, neutral, global standard has been growing steadily and now has more than 60 corporate members and 48 associate members. Corporate members include PCB design and supply chain companies from PCB ECAD companies such as Altium, Cadence Design Systems, Mentor Graphics, Zuken, ADIVA, Downstream, and WISE Software, to name a few. Members also include companies that provide software to EMS, fabrication and contract manufacturers such as AEGIS, Cimnet, Direct Logix, Easy Logix, GraphiCode, and Polar Instruments. Other members are EMS providers, contract manufacturers, fabrication companies, and IPC.

Unprecedented Collaboration

The IPC-2581 Consortium has achieved unprecedented collaboration between PCB design and supply chain companies. When the consortium was founded, there were several initial challenges. Through collaboration, the consortium has:

- Developed software to export/import IPC-2581 data
- Developed methods to test and validate data generated by software companies
- Created an initial set of publicly available sample test cases
- Conducted multiple three-way meetings between a design house, their ECAD supplier and their fabrication/manufacturing suppliers
- Identified areas in the 2581 specification that were ambiguous, design and implement changes to clarify the spec
- Identified improvements needed to make the data hand-off even more efficient

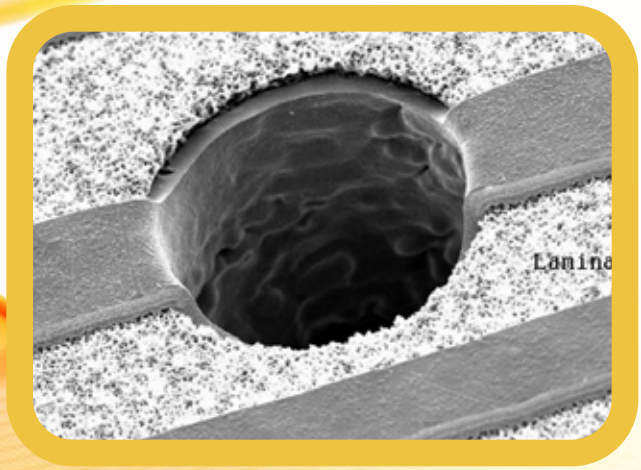
We deliver Advanced PCB Solutions!



Fine line PCB, 2 mil line /space

We have developed a unique set of processes based on electro-depositable liquid photoresist.

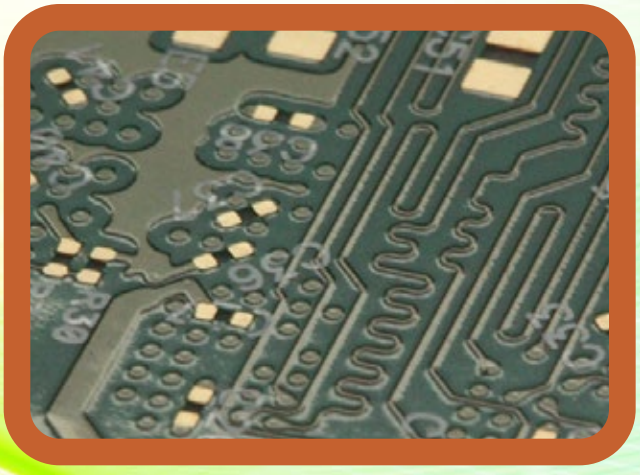
CLICK TO LEARN MORE



Landless Via Technology

We're the only manufacturer in the world to have perfected a liquid photo-imageable resist (PiP) in electrolytic form, used for all our production.

CLICK TO LEARN MORE



Impedance Tolerance <5%!

With our panel plating process combined with continuous foil lamination, our impedance tolerances are second to none!

CLICK TO LEARN MORE

Our unique processes enable us to create and deliver Advanced PCB Solutions that meet the needs of the demanding market at competitive prices!

CANDOR INDUSTRIES, INC.

ADVANCED PCB SOLUTIONS

www.candorind.com | sales@candorind.com | (416) 736-6306

IPC-2581 ADOPTION UPDATE *continues*

Figure 1: Corporate members of the IPC-2581 Consortium.

Several design bureaus within the consortium ran their own internal tests to validate IPC-2581 output from their ECAD tools. They partnered with their ECAD and manufacturing partners to resolve any issues that came up during their validation process. Often design bureaus would compare traditional outputs (Gerber, ODB++) with IPC-2581 data. Cisco Systems reported that they are evaluating 51 current production designs of various technologies. They also reported excellent support and collaboration between their ECAD and manufacturing partners and are in the process of updating their internal stack-up generator tool to support 2581 input and output.

This industry-wide collaboration led to the fastest revision of a standard in IPC history. The consortium, in partnership with IPC, developed IPC-2581 revision B in 12–14 months, from identifying the list of changes needed to sending the specifications out for ballot approval by IPC members.

Revision B of IPC-2581 Enhancements include:

• Assembly data: Library pin 1 orientation, primary pin tag, pickup point for components, polarity markings. Library orientation data provides the assembly process a key to zero orientation of device in the design relative to zero orientation of assembly equipment. The orientation options are based on the different library standards across the globe.

The "Pin one" attribute identifies the primary pin of a package to identify the key pin for placement verification and other processes with the fabrication, assembly and test processes. Various optical inspection tools for assembly verification can use an attribute associated with graphical object, such as the "+" polarity marking in silkscreen or copper.

• Bill of material (BOM) updates include: Enterprise data (person, role, design revision, history, software etc), instance-based footprint reference, variant design support and enhancements to stack-up definitions. The enterprise data embedded into the IPC-2581 file contain contact information, BOM revision data, board revision data and

INTRODUCING COOLSPAN® TECA

thermally & electrically conductive adhesive

Rogers can help by being your reliable conductive adhesive film source

Get the heat out of those high-power PCBs. COOLSPAN® Thermally & Electrically Conductive Adhesive (TECA) Films are ideal for dissipating heat in high-frequency circuits. COOLSPAN adhesives feature outstanding thermal conductivity (6 W/m/K) and reliable thermal stability. Keep things cool, with Rogers and COOLSPAN TECA film.

CONTACT YOUR SUPPORT TEAM TODAY

ROGERS CORPORATION

www.rogerscorp.com

MEET YOUR COOLSPAN® TECA FILM SUPPORT TEAM

Leading the way in...

• Support • Service • Knowledge • Reputation

SCAN THE CODE TO GET OUR CONTACT INFO.

Greg Bull
Applications Development Manager
Northern Territory (U.S.) & Canada

Dale Doyle
Applications Development Manager
Western Territory (U.S.)

John Dobrick
Applications Development Manager
Southern Territory (U.S.) & South America

Scott Kennedy
Applications Development Manager
Eastern Territory (U.S.)

John Hendricks
Regional Sales Manager
Europe

Kent Yeung
Regional Sales Director
Asia

If you are unable to scan a VR code please visit our Support Team website at www.rogerscorp.com/coolspan

IPC-2581 ADOPTION UPDATE *continues*

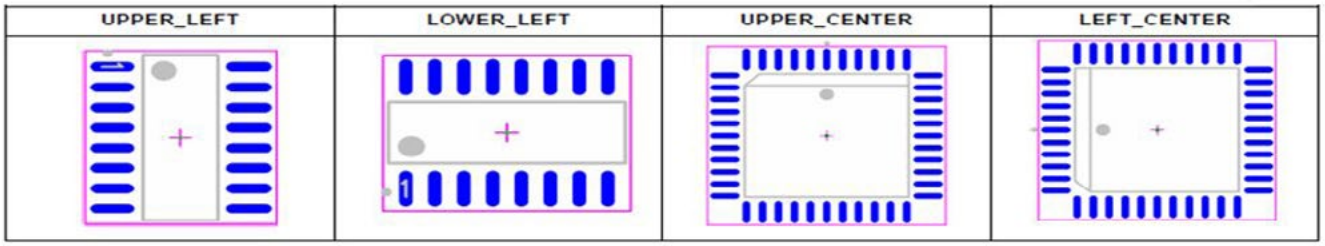


Figure 2: Rev B allows use of attributes associated with graphical objects, such as the "+" polarity marking.

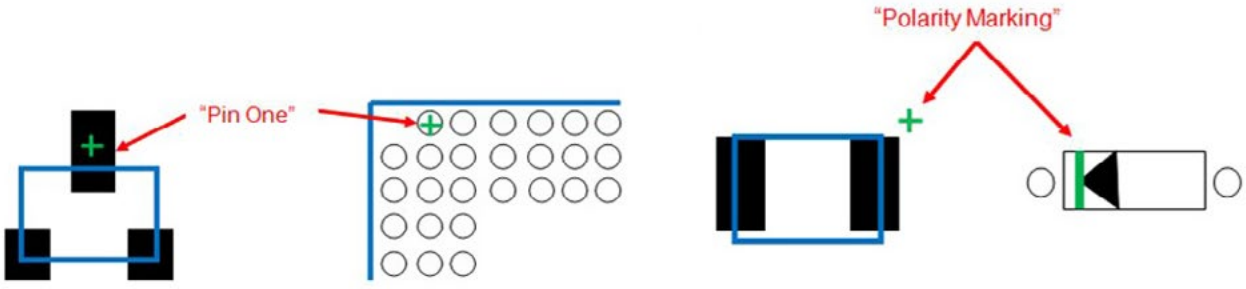


Figure 3: a) Library Pin one orientation, b) Pin One/Primary Pin marking, c) Polarity marking.

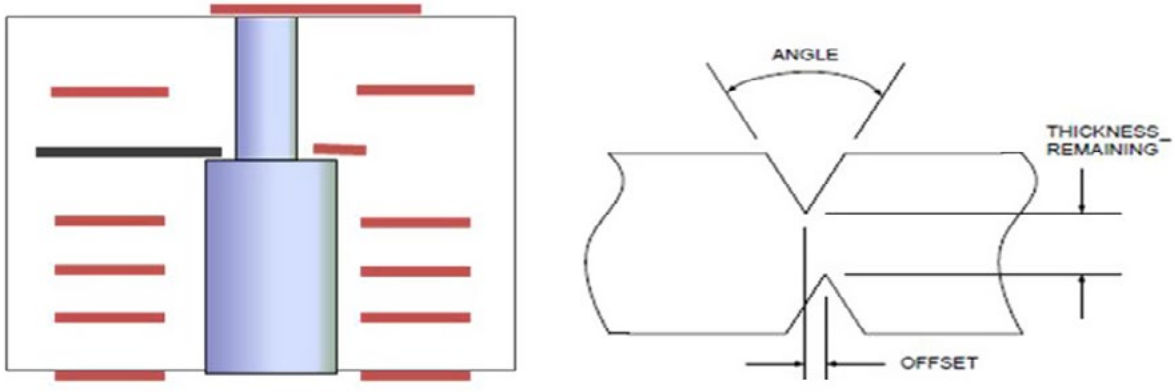


Figure 4: a) Backdrilling of a via stub, b) V-groove parameters within IPC-2581 revision B.

links to specific software for FPGAs as an example.

• Drill-related improvements: Specific descriptions for slots and cavities (depth, tolerance, plating), Backdrill data attributes (size, tolerance, start, do not cut layer, max stub length), V-cut/V- grove (angle, offset, thickness, tolerance) for panel and pallet construction.

• The SPEC (specification) section enhancements provide a SPEC dictionary. SPEC defines design intent and can be attached to objects in the design. This will associate currently specified fabrication/assembly notes to the specific objects. The SPEC definition could describe a specific requirement for a part during the assembly process that would typically be described in the assembly drawing. The SPEC definition in IPC-2581 would allow that note to be attached to the component instance and reference electronically, rather than shuffling through paper documents. SPEC has a very wide usage within IPC-2581 as fabrication/assembly notes are embedded directly into the IPC-2581 file.

• Last, but not the least, a set of enhance-

MIRACO

Engineering And Providing Balanced Interconnect Solutions

Flexible Printed Circuits • Rigid Flex • Wire Harnesses • Complete Assemblies

Our products and services are specifically designed to empower our customers to produce a product with superior performance and quality, as well as lower design, assembly, and system installation costs.

Partnering With Your Engineering Team To Deliver The Best Solution

...connecting technology

Miraco, Inc. • 102 Maple Street, Manchester, NH 03103 • miracoinc.com
603-665-9449 • Fax: 603-665-9459

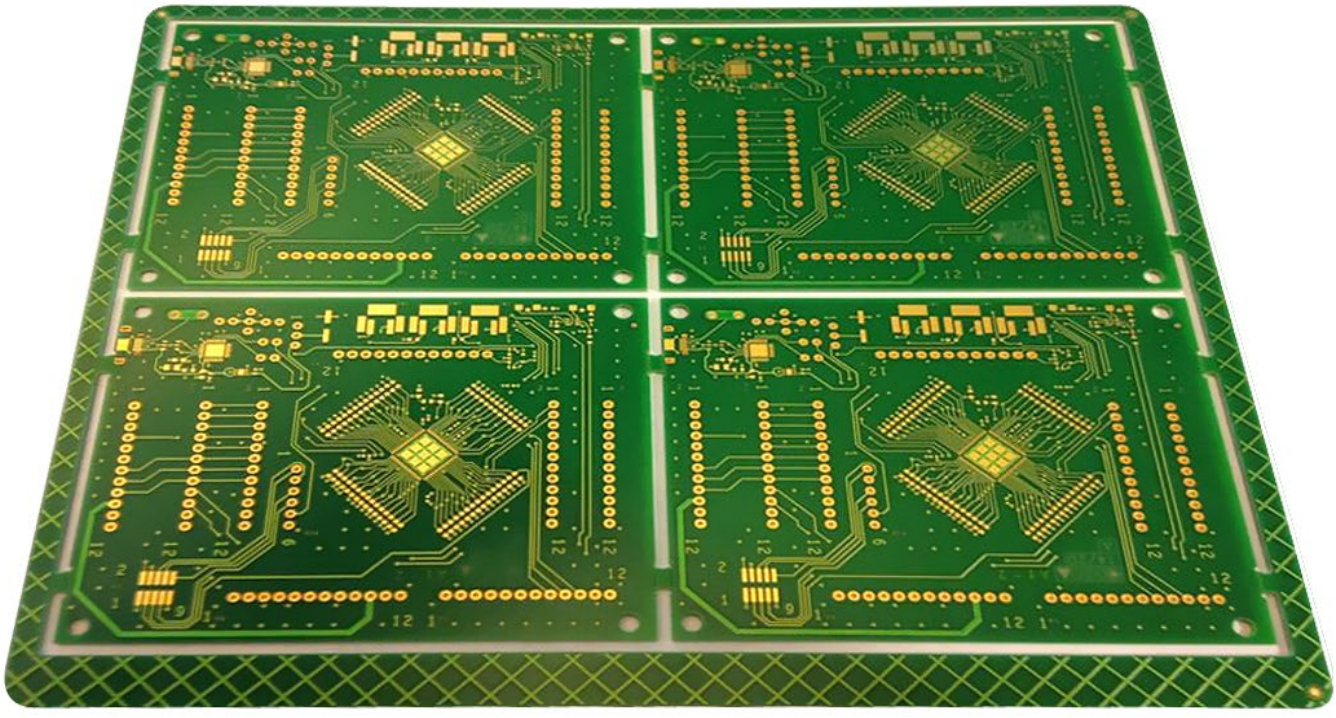


Figure 5: Image of PCB successfully built by Vellux.

ments includes an expanded definition of the stack-up. This enhancement exemplifies the innovation that the Consortium collaboration has achieved.

IPC-2581 rev B Stack-up Exchange

The idea behind enhancing the stack-up definition within IPC-2581 was simple, yet brilliant. As we all know, for many designs with high-speed requirements, design bureaus send their requirements to their fabrication/manufacturing partner, such as achieving 75 ohms on a certain layer. The fabricator sends a suggested layer stack-up for review and approval. This collaboration happens today with spreadsheets, Microsoft PowerPoint, Microsoft Word documents and a few phone calls. The suggested stack-up is entered into the PCB layout tools manually (painfully). Any disconnect between the fabricator and the design bureau is not discovered until after the design is completed. Last-minute changes to a completed design can be very time-consuming and painful.

With IPC-2581 rev B, the design bureau and fabricator can exchange the proposed stack-up electronically, and since it can be consumed by the PCB design tools, it saves a lot of time entering the data into the PCB CAD tools. More importantly, there is little chance of introducing errors in the process. The stack-up definition has the capabilities to describe a stack-up in a designer's perspective or from a manufacturer's perspective. A design view may show a basic view of a stack-up, and a manufacturer's view may display the multiple materials to make up a dielectric or core layer build up. BOM references for the stack-up materials are also built into the IPC-2581 data.

Adoption

The consortium launched with 11 founding members and has grown steadily over the past two years with more than 60 members today. Consortium members have built boards using IPC-2581 through several manufacturing companies.

Figure 8 depicts the latest support status for IPC-2581, which is updated on the consortium website on a regular basis.

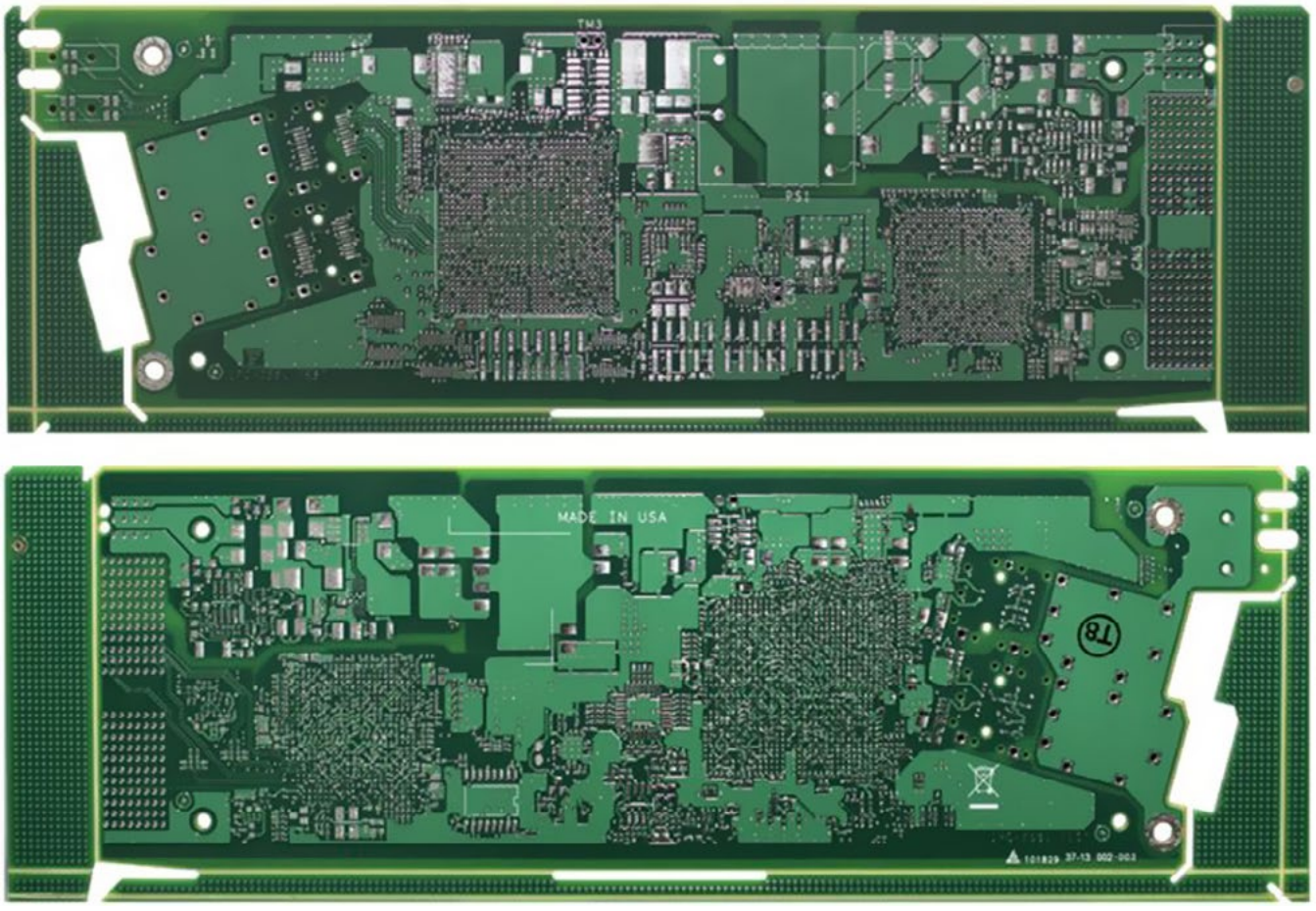


Figure 6: Fujitsu Network Communications PCB fabricated using IPC-2581 by Sierra Circuits using Frontline Genesis 10.2 software.

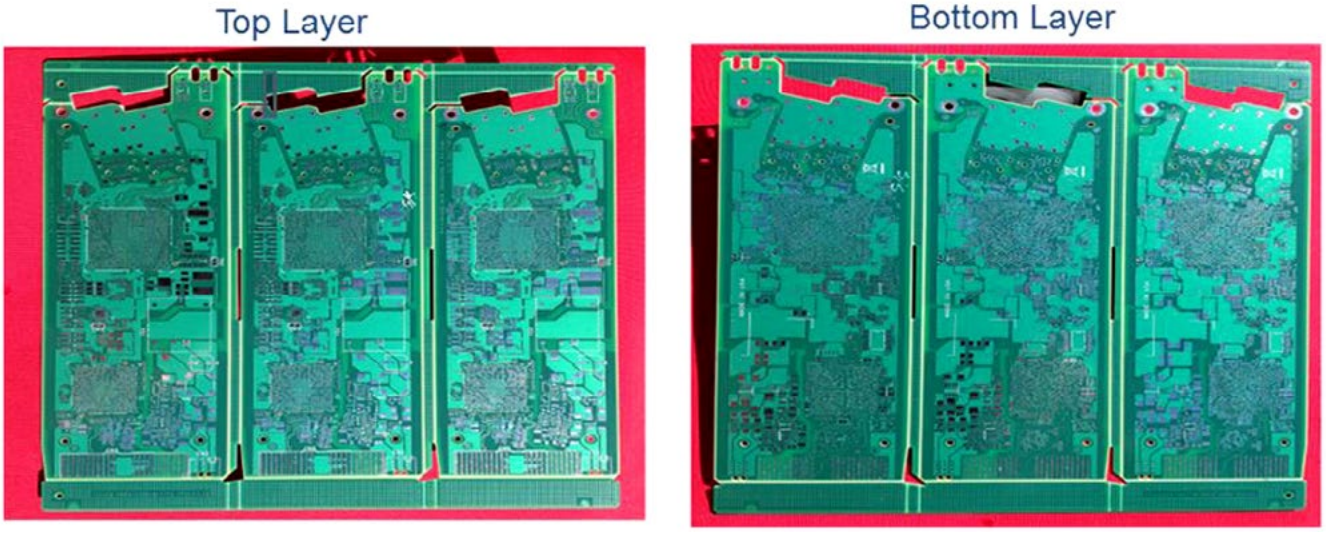


Figure 7: Fujitsu Network Communications PCB fabricated using IPC-2581 by Sanmina-SCI using Frontline Genesis 10.2 software.

IPC-2581 ADOPTION UPDATE *continues*

Manufacturer Support Status

Company Name	Software Used	IPC-2581 Amend 1	IPC-2581A	IPC-2581B	Stack-up Exchange
Accurate Circuit Engineering	Genesis, InSight, InPlan		•		
Axiom	VisualCAM	•	•	•	•
	CircuitCAM		•	Q4 2014	
CC Electronics	VisualCAM	•	•	•	•
Electrostein	CAM350	•	•	•	
Sanmina	Genesis, InSight, InCAM		•		Q4 2014
Sierra Circuits	Genesis		•		
Viasystems	Genesis		•		

Software Vendor Support Status

Company Name	Software Name	IPC-2581	IPC-2581A	IPC-2581B	Stack-up
AEGIS	Factory Logix	•	•		
ADIVA	ADIVAnet	•	•	•	
	ADIVADRC	•	•	•	
	ADIVAview	•	•	•	
Altium	Altium Designer			Q3 2014	
Cadence	Allegro PCB Designer	•	•	•	•
	OrCAD PCB Designer	•	•	•	
Downstream Technologies	CAM350		•	2014	
	Blueprint PCB		•	•	
	DFMStream		•	2014	
EasyLogix	PCB-Investigator	•	•		
In-Circuit Design	ICD Stackup Planner		•	2014	2014
Numerical Innovations	FAB 3000 Version		•		
	ACE 3000 Version		•		
	PreflightPCB Version		•		
Polar Instruments	Speedstack			•	•
PTC	PTC Creo View ECAD		•	Q3 2015	
Siemens	Test Expert		•	•	
	UniCam FX		•	•	
	UniDoc FX		•	•	
Vayo	VayoPro-DFM Expert		•	2014	
	VayoPro-SMT Expert		•	2014	
	VayoPro-Test Expert		•	2014	
	VayoPro-Document Expert		•	2014	
	VayoPro-View Expert		•	2014	
WISE	VisualCAM	•	•	•	•
	GerbTool	•	•	•	
	WISE2581Viewer	•	•	•	•
Zuken	CR-5000	•			
	CR-8000	•		Q1 2015	

Figure 8: IPC-2581 support status: IPC-2581A widely supported by the majority of the software suppliers. Software vendors are also gearing up to support IPC-2581 revision B.

Join This Industry-Changing Process

You can be part of this exciting, industry-changing process—you can learn, participate and contribute. You can be the IPC-2581 expert within your company!

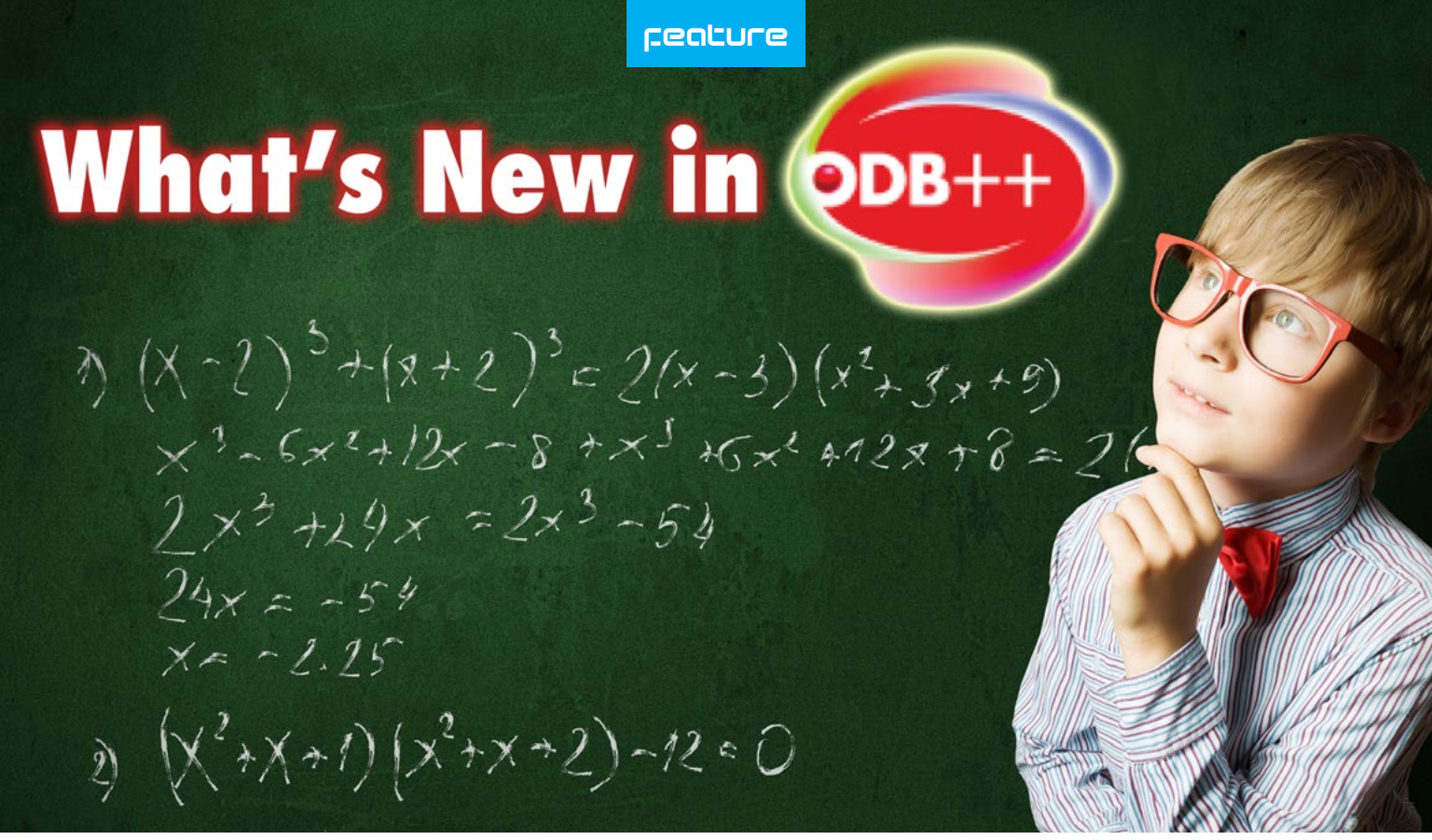
- Sign up as a consortium associate member and learn more about improvements being made to the standard through consortium efforts
- Get your company to join the consortium as a corporate member
  - Leverage the expertise in the consortium's technical team to do a deep dive in the technical aspects of the specification
  - Use your PCB design software now to generate and send IPC-2581 to your suppliers. Let them know that this is the future of your release package for PCB manufacturing – an intelligent, open, neutral data format with everything in one file
  - Leverage the consortium members to help your suppliers come up to speed on IPC-2581

Visit www.ipc2581.com to join, and start your wonderful journey with the consortium members. **PCBDESIGN**

Hemant Shah is IPC-2581 Consortium chair and product management group director for Allegro PCB products with Cadence Design Systems.

Ed Acheson is the IPC-2581 technical committee chair and principal product engineer for Allegro PCB products with Cadence Design Systems.

What's New in ODB++



by Julian Coates
VALOR DIVISION, MENTOR GRAPHICS

ODB++ is a complete PCB manufacturing exchange data format that contains all of the data required for defining a PCB product in manufacturing. "ODB" stands for Open Data Base, with the format openly available to anyone who registers as a member of the ODB++ Solutions Alliance.

All of the fabrication requirements such as the graphical definition of the layers or mechanical information, the underlying data represented in drawings such as the drill drawings, fabrication instructions, layer buildup definition, and also the information required for bare-board testing and automatic optical inspection are included in the ODB++ product model. For PCB assembly, all of the manufacturing information is included: the solder paste definitions, the component placements and rotations, the BOM, and the approved vendor list for alternative parts, as well as the ICT test-point locations. All the product model content is contained within a simple archive that can be sent to those in the manufacturing supply chain.

In the newest version of ODB++, v8, content has been added based on input received from the thousands of people who use ODB++ and solutions-development partners worldwide, either directly or through the technical support channels of CAD/CAM tool vendors. Version 8 contains significant incremental improvements over the current mainstream version (ODB++ v7), and is designed to enable a smooth transition to higher levels of process integration and automation across the design/fabrication/assembly/test PCB flow.

ODB++ v8 enables software tools such as DFM analysis and CAM systems to perform their tasks with the minimum dependency on keyboard/mouse input and the maximum level of automation based on the intelligence embedded in the software-model of the PCB product.

What's Contained in an ODB++ Product Model

Within any ODB++ product model are the PCB Steps. Originating from the term "step and repeat," the ODB++ Step is a container for all the elements required for a PCB object. A Step can be a single PCB object, an assembly panel object, or a fabrication panel object containing a number of assembly panels.

Living proof that flying dragons are real!

Dragon Circuits is proud to be at the forefront in unmanned aviation.

Interested in unmanned aerial or ground vehicles? Dragon Circuits is developing the newest technology to enhance vehicle run-time, performance and durability to put your company at the top of the industry. Proprietary electronics, built in the USA with ITAR, AS9100 and MIL-SPEC standards. Contact us for more information on a range of services from design, manufacturing, and even flight school!

LEARN MORE »

DRAGON CIRCUITS

www.dragoncircuits.com | 972.790.7610

WHAT'S NEW IN ODB++? *continues*

It includes the PCB product matrix that defines all of the layers required for the PCB with their signal layers, power and ground layers or mixed layers, and the solder mask and solder paste layers…all listed in the correct order. Component layers are added for the top and bottom sides of the PCB, and all of the drill pairing information is included. Specific layers for routing and v-scoring information as well as documentation layers are included.

Because all of this information is included in ODB++, a build-up drawing is not needed to define the layer stack. All of the physical layers detail is included such as the legend layer used during the silk-screening process, the solder mask layers for both top and bottom sides of the board, as well as all of the copper layers required together with their thicknesses/weights and foil/laminate variations. This means that Gerber files, a listing of the layers, or any other readme files do not need to be sent to the PCB manufacturers, as traditionally would be done.

All of the drill-pair layer information is included, and for each one of those drill-pairs layers, we have a drill tool layer that includes all of the drills needed for that drill pairing and includes the finished drill size as well as the type of hole, whether it is plated or non-plated, or maybe a via. This means there is no need to supply Excellon drill files, drill drawing, or any drill table to define the drilling information because it is self-contained in the ODB++ product model.

Often, a netlist needs to be sent to PCB fabricators so they can perform bare board tests. ODB++ contains netlist information. The netlist is generated directly from the PCB CAD system that contains all of the functional net names. ODB++ contains a second netlist derived directly from the copper features and the drill interconnects, and this netlist can be used to drive the bare-board test.

The component layers are included in the PCB product matrix, and they carry all the

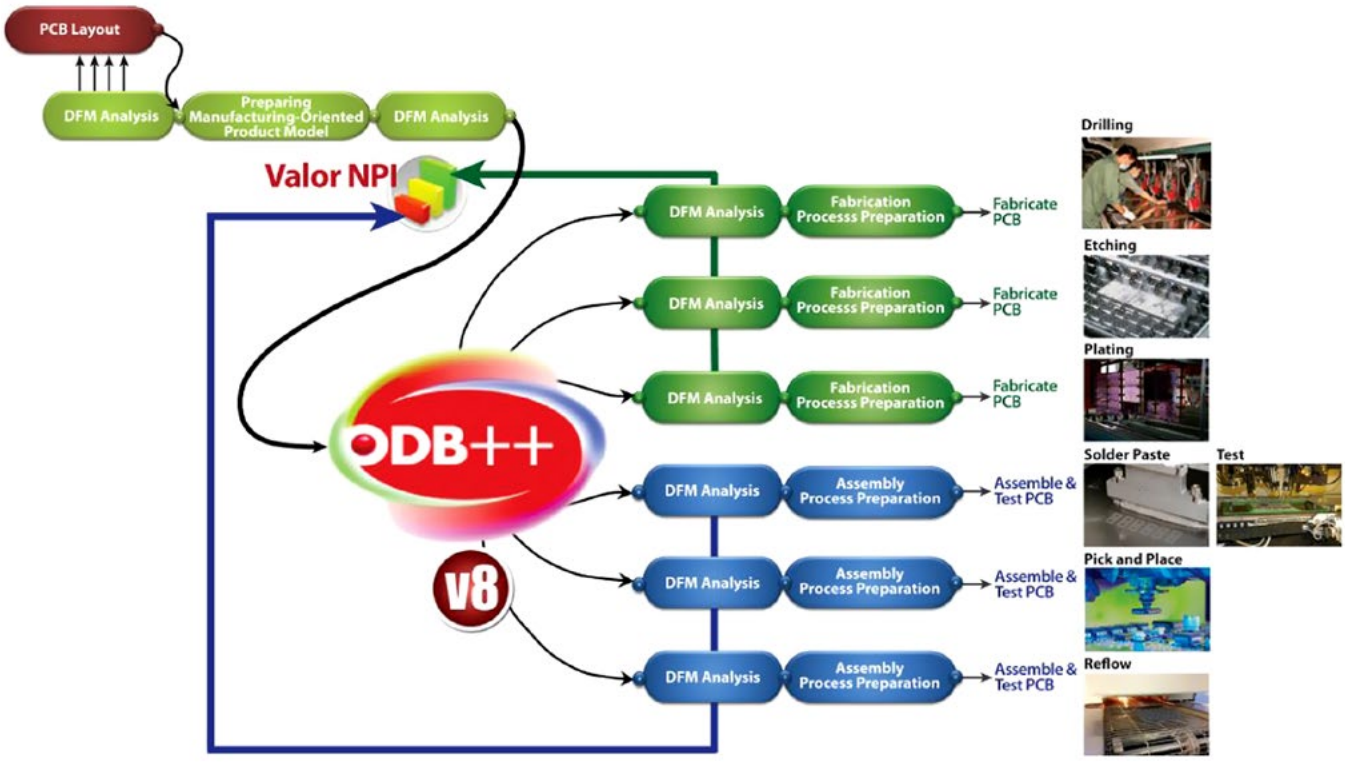


Figure 1: Manufacturing processes to consider in PCB layout design for fabrication are the drilling process, etching, and galvanic plating processes. For assembly operations, key processes to consider include solder paste printing, placement, reflow, and test.

component placement information required for pick-and-place during assembly. ODB++ also includes the reference designators, along with x and y coordinates, rotations, and placement side. This removes the need for any separate assembly drawings, pick-and-place files, or assembly instructions as a way of conveying the product model into process-preparation.

The ODB++ product model also contains the BOM that includes reference designators, the manufacturer names, manufacturers' part numbers, and the quantities. In the case of an approved-vendor list, alternative manufacturer names and part numbers can be included if more than one manufacturer's part can be used.

ODB++ is a working solution that has been used for millions of PCB designs across global supply-chains, and adoption is growing daily.

"Traditional stackup drawings can be eliminated from the flow, thus avoiding the steps of producing the drawing, reading the drawing, and typing the data back into the CAM system at the manufacturing level."

New in ODB++ v8

The following is a summary of the new items in the latest version of ODB++, v8, as well as implementation recommendations.

Changes to PCB Structure Information

The PCB structure allows explicit modeling of flexible and flex-rigid PCB structures. By including an exact definition for entities such as covercoats, coverlays, stiffeners, bend radius, etc., DFM analysis functions can be automated to new levels for flex and flex-rigid designs. Following DFM, the manufacturing process can be derived more automatically based on the embedded intelligence.

Multilayer PCB build-up information is stored in the product model. Traditional stackup drawings can be eliminated from the flow, thus avoiding the steps of producing the drawing, reading the drawing, and typing the data back into the CAM system at the manufacturing level. This is designed to save time and reduce errors. It allows delivery of the multilayer build-up information directly into the fabricator's material selection and stack-up validation processes.

This version fully implements metric units, meaning that all aspects of the PCB product model, not just the feature coordinates, can be expressed in metric units. ODB++ now has equal value to engineering processes that use either the metric or imperial measurement systems.

In ODB++ v8, DFM analysis can take into account the direction of drilling, which allows more accurate DFM analysis of buried and blind vias, back-drilled holes, and holes drilled with multiple diameters.

A profile with holes can be created, which gives a more efficient definition of the PCB profile, requiring fewer layers of data for the complete definition.

Feature-Level Improvements

Attributes are now fully independent of any software application, and have been categorized according to their primary purpose—whether to support DFM analysis, to define the product-model, or to define the intended manufacturing process (split by fabrication, assembly, test, generic). This categorization supports a wider use of the attributes-intelligence across the design/manufacturing flow, thus enabling higher engineering automation overall.

The new version has an expanded range of standard symbols, developed particularly for the purpose of designing solder-stencil openings. With the introduction of all standard symbols known to be needed by the solder-stencil process, ODB++ v8 enables fully automated solder-stencil design based on manufacturing process rules. Those who are using it no longer have to create and maintain their own libraries of custom symbols.

The net name length has been enlarged (unlimited length). In all circumstances, net-names can be preserved across the design/manufac-

turing flow, thus enabling effective net-related engineering collaboration based on the ODB++ data, even with the most complex PCBs.

Assembly and Test Improvements

ODB++ v8 supports definition of structural test probes. The test probe diameter attribute provides information on the size of test probes. This enables the definition and DFT validation of physical test-access early in the design stage, thus avoiding the need to redefine at the assembly stage. It provides the means for explicit transmission of test intentions from design to manufacturing.

An unlimited number of BOM description attributes is now supported, which means there is no loss of component description data across the flow. This reduces the need for multiple BOM access points in the flow just to recover data lost during the BOM-parsing process.

The introduction of package attributes enables DFM analysis and manufacturing process preparation functions to be based on package type, which allows more efficient processing of the product model.

Bridging the Design-Manufacturing Gap

ODB++ has been implemented in the software of all leading CAD/CAM-solution vendors. The latest version of ODB++ enables the comprehensive flow of critical structured data files between PCB layout design and PCB manufacturing disciplines. For example, with Valor NPI using ODB++ version 8, DFM analysis can be run concurrently at milestones during the PCB layout design. This process is compatible with PCB design tools such as Mentor Graphics' Xpedition and PADS, Cadence Allegro, Zuken CR5000 and CR8000, and Altium.

ODB++ v8 Enables Lean NPI Flow

In a Lean NPI flow, the final manufacturing outputs are derived directly from the master ODB++ data that was used all along the way

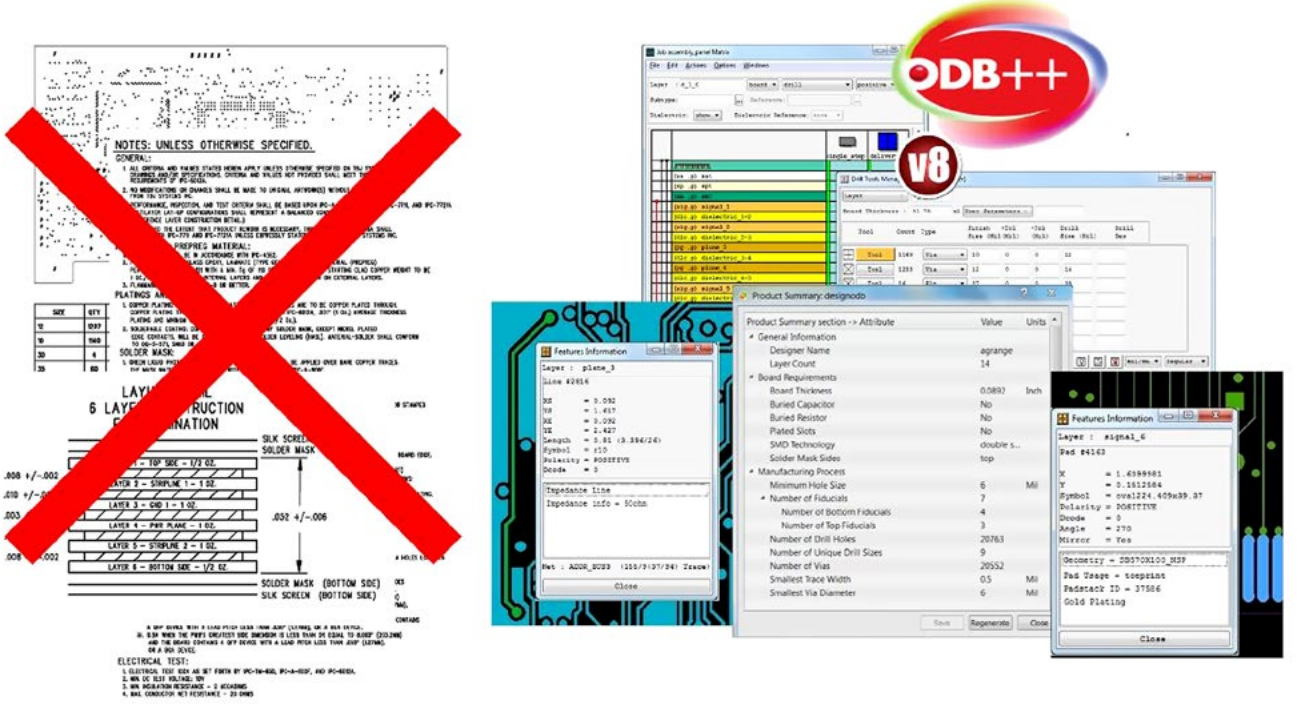


Figure 2: When a complete Lean product-new product introduction (NPI) is done, the ODB++ product model is much more than just an alternative to Gerber. It delivers a complete definition of what has to be manufactured, including all of the information traditionally carried in paper or PDF documents, integrated into the structured data ready for immediate and automatic use by the next software tools in the flow.

through the Lean, integrated product- and process-NPI stages. Depending on the exact manufacturing machinery to be used, the data output can be modified to suit.

In the best-practice Lean NPI flow, the manufacturing-level product model in ODB++ format includes a fully constructed and verified assembly panel in one structured data file. From this master product model file, combined with a defined manufacturing process definition, the manufacturing-process data can be automatically generated for fabrication, assembly, and test. This makes the NPI process much faster, while reducing the possibility for error and lowering the risk.

Anyone who would like to get involved with the ODB++ Solutions Alliance is welcome to join. Visit www.odb-sa.com. **PCBDESIGN**

Julian Coates is the director of business development for Mentor Graphics Valor division. Since joining Mentor Graphics Valor division in 1994, Coates has fulfilled a number of roles including managing director of Valor's European subsidiary, followed by product management, marketing and business development.

New X-ray Imaging Allows Monitoring of Treatment

Scientists have developed an X-ray imaging system that enables researchers to see "live" how effective treatments are for cystic fibrosis.

Published in the American Journal of Respiratory and Critical Care Medicine, the imaging method allows researchers to monitor the effectiveness of a treatment for the life-threatening genetic disorder.

Dr. Kaye Morgan, lead researcher on the paper from Monash University, said the new X-ray imaging method allows researchers to look at soft tissue structures, for example the brain, airways and lungs, which are effectively invisible in conventional X-ray images.

"At the moment we typically need to wait for a cystic fibrosis treatment to have an effect on lung health, measured by either a lung CT scan or breath measurement, to see how effective that treatment is," Dr. Morgan said.

"However the new imaging method allows us for the first time to non-invasively see how the treatment is working 'live' on the airway surface."

Dr. Morgan said this X-ray imaging method would enable doctors and researchers to measure how effective treatments are, and progress new treatments to the clinic at a much quicker rate, a key goal of co-authors Dr. Martin Donnelley and Dr. David Parsons of the CF Gene Therapy group at the Women's and Children's Hospital and the University of Adelaide's Robinson Research Institute.

"Because we will be able to see how effectively treatments are working straight away, we'll be able to develop new treatments a lot more quickly, and help better treat people with cystic fibrosis," Dr. Morgan said.

Dr. Morgan said the new imaging method, which was developed using a synchrotron X-ray source, may also open up possibilities in assessing how effective treatments were for other lung, heart and brain diseases.

PCB007 News Highlights

Viasystems' PCB Segment: Q2 Shows Improvement

"Second quarter results in our PCB segment reflect improvement in most of our end markets, both sequentially and year-over-year," noted CEO David M. Sindelar. However, we are still facing inconsistent customer project demand for our electromechanical solutions product offerings, which is included in our assembly segment."

Spirit Circuits to Acquire Teknoflex Equipment

Sadly, trading conditions and tough competition have resulted in the demise of one the UK's longest-established flexible PCB manufacturers. Although confidence in UK manufacturing is growing, this highlights the challenges being faced by many businesses that rely on a single product offering and that do not diversify and embrace trading with offshore suppliers.

Exception PCB's Neil Day Awarded CID Certificate

Design Manager Neil Day has completed the IPC CID training course and attained CID certification. Training was completed at the PIEK International Education Centre in The Netherlands under the tutorage of Rob Walls and is a significant investment in the design service from Exception PCB Solutions.

IPC: N.A. PCB B2B Ratio Returns to Parity in June

"The PCB book-to-bill ratio has been hovering around 1.00 since February, which explains the flat year-to-date sales growth we are seeing," said Sharon Starr, IPC's director of market research. "This month's growth in orders is a positive sign, however, and if it continues we can expect to see sales improve later this year."

Wurth Elektronik Embraces Modern Data Formats

A new generation of PCB data formats enable a better exchange of data between CAD and CAM. The ODB++ and IPC-2581 formats include not only the graphical information for the individual board layers, but a lot of important extra information as well. All of the data required for manufacturing, testing, and assembly are contained in one file.

WUS Invests in Schweizer; Acquires 4.5% Stake

Following the exclusive, long-term strategic alliance for the high frequency (HF) segment, WUS Printed Circuits Co., Ltd. and Schweizer Electronic AG agreed on a capital transaction with WUS acquiring 4.5% of Schweizer's shares.

HEI Reports 39% Sales Drop in Q2

HEI, Inc. has announced unaudited financial results for the second quarter of 2014, which ended June 28, 2014. Sales in the second quarter of 2014 were $7,940,000, compared to $13,018,000 in the second quarter of 2013. The company generated a net loss of ($429,000) in the second quarter of 2014, compared to a net income of $678,000 in the second quarter of 2013.

Wurth Elektronik Combines Rigid-flex, Impedance Testing

When calculating the impedances in rigid-flex printed circuit boards, the rigid and the flexible area must be considered separately. The cause of this is the differing signal behavior due to the surrounding materials. Würth Elektronik uses a special software that calculates everything one step.

MFLEX Completes Restructuring, Expecting Growth in Q4

"At the mid-point of our guidance range, we expect to generate breakeven net income, excluding impairment and restructuring. With our improved cost structure in place, we should see a continued recovery in our profitability as we leverage anticipated stronger sales volume," said Reza Meshgin, CEO.

AT&S Posts Positive Q1 FY 2014/15 Results

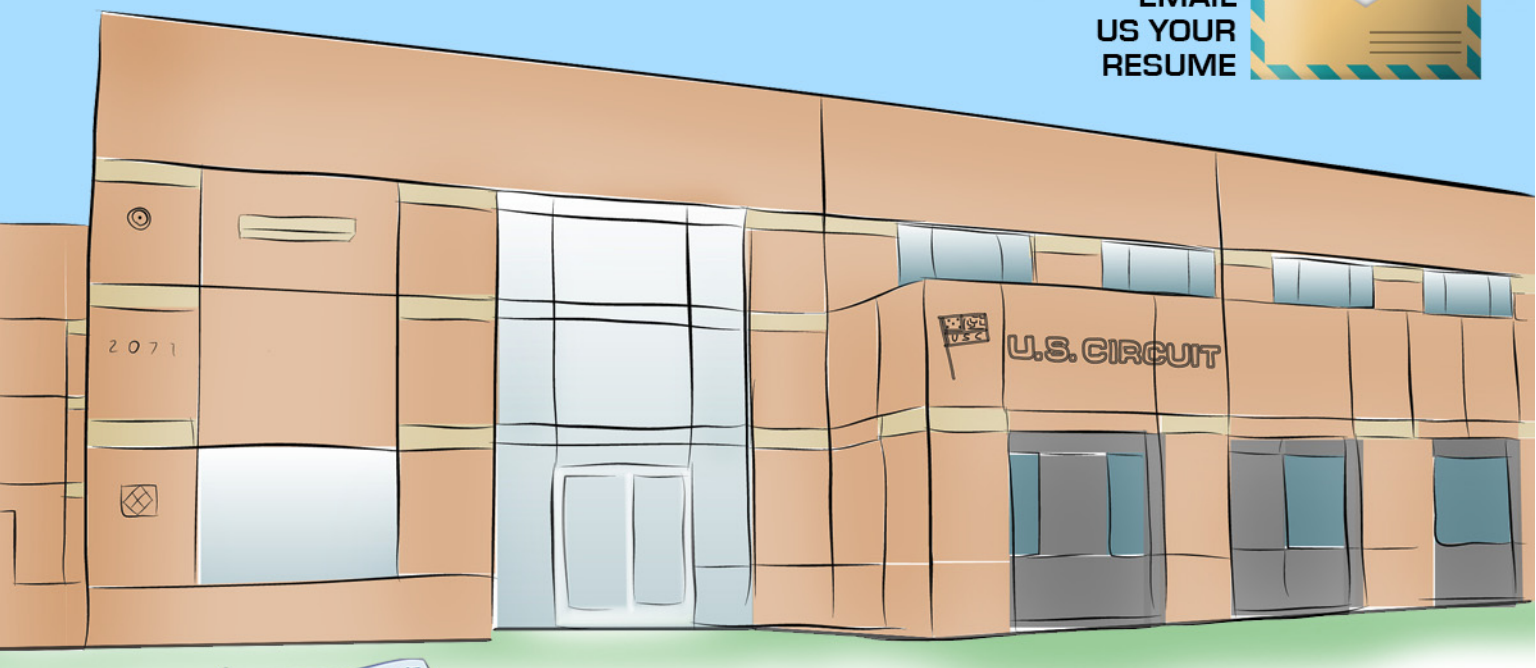
The AT&S Group generated revenue of Euro 141.3 million in the first three months of the financial year, which was in line with the previous year's total (Q1 2013/14 Euro 142.5 million). Earnings before interest EBITDA amounted to Euro 29.1 million, an increase of 3.6%. Consolidated net income for the first quarter rose by 14.6%.

NOW HIRING

Outside Sales Representative

We are looking for a highly motivated, independent individual to help us build a customer base in the US. We are a quick-turn and production, high-low mixed technology, bare board manufacturer. Qualifications include: Knowledgeable with PCBs; Sales experience required; Strongly motivated to succeed.

EMAIL US YOUR RESUME



U.S. CIRCUIT

U. S. Circuit, Incorporated
2071 Wineridge Place
Escondido, CA 92029
Ph: (760) 489-1413
Fax: (760) 489-2965
www.uscircuit.com

Superior Quality
Superior Service

Call for a Quote: (760) 489-1413 or
email: rsojitra@uscircuit.com

ITAR Registered | ISO 9001:2008 | MIL-PRF-55110G

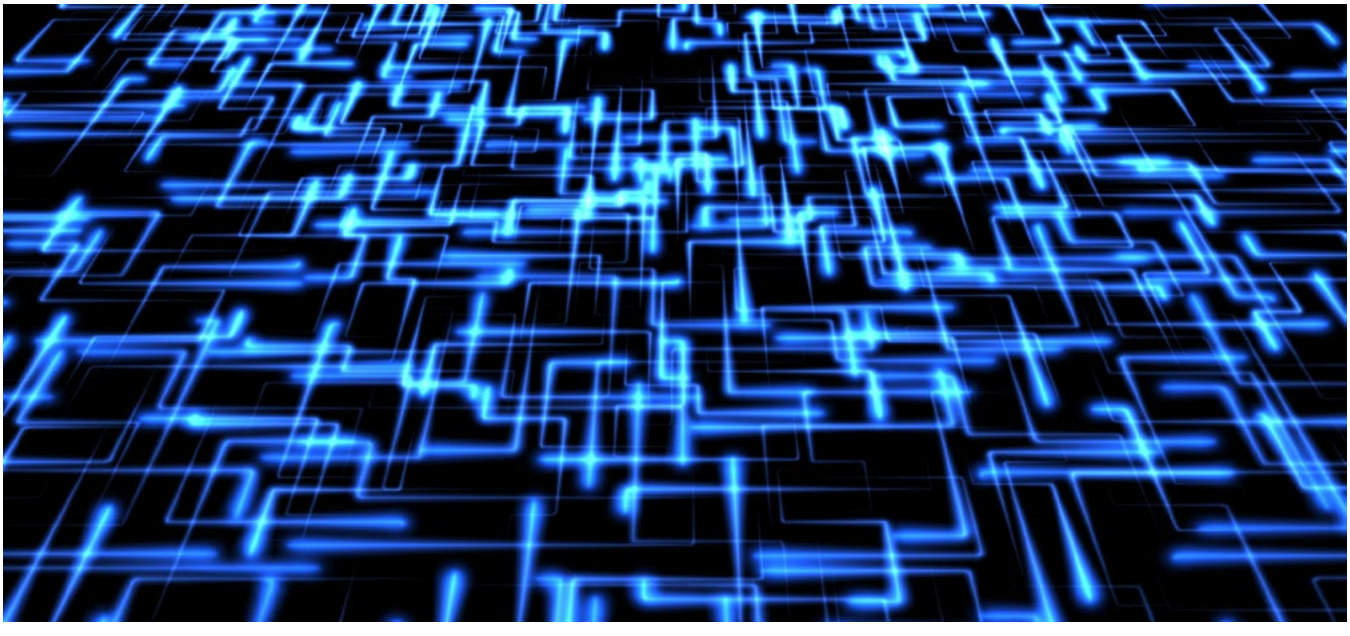
IPC-2581B Eases Stackup Development

by Amit Bahl
SIERRA CIRCUITS

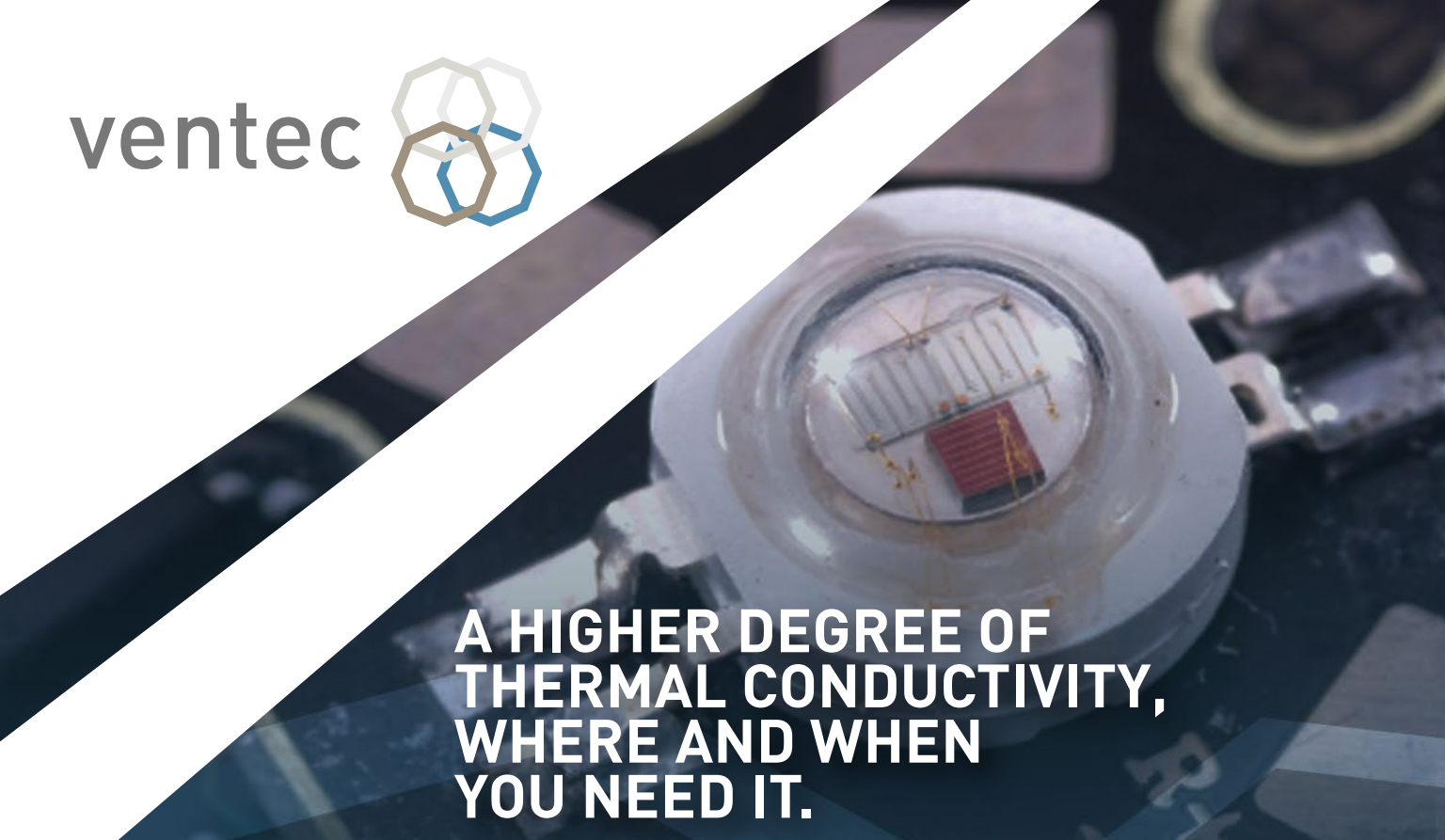
PCB manufacturers often find that important details are unclear or missing from the designs that customers submit, and such projects can't move forward until the designers are reached for clarification. In many of those cases, it is the way design data are organized and conveyed that is ultimately to blame.

Whatever the EDA platforms that were used to create them, most PCB designs are output and sent to manufacturers as a collection of Gerber files that graphically define the layers, a drill file, a netlist, a board drawing including the stackup, and a readme text of notes and instructions. Turnkey orders for combined fabrication and assembly also include a BOM file and coordinate data for pick-and-place operations. There is no common data format among all the files: They're simply bundled together and forwarded to the manufacturer to download and interpret. And that disparity among formats can lead to omissions on the design side and miscommunication with manufacturers.

Now consider what occurs (or should occur) long before any complex design is completed and sent for fabrication. The initial design step leading to a successful PCB layout for any complex, high-speed circuit is close consultation with your manufacturer to determine the optimum stackup. The process is iterative, a back-and-forth collaboration to select the right materials; determine line widths, spacings, and layer thicknesses to meet impedance values; and minimize the number of layers and nail down the via set within budget. Here again, there's no common protocol for how that's accomplished. The process involves telephone calls, drawings, and emails until consensus. On one hand, there's stackup information the designer will use as the foundation for the layout. On the other hand, there's a detailed stackup from a manufacturing perspective, which describes how each layer will be constructed, and if the design will involve sequential laminations, how the layers will be grouped for fabrication.



ventec



A HIGHER DEGREE OF THERMAL CONDUCTIVITY, WHERE AND WHEN YOU NEED IT.

	Thermal Conductivity	Ceramic Filled	Fully Formable	Non-Glass Reinforced	Halogen Free
VT-44A	1.0W/m.K.	✔			
VT-4A1	1.6W/m.K.	✔			
VT-4A2	2.2W/m.K.	✔			
VT-4B1	1.0W/m.K.	✔	✔	✔	✔
VT-4B3	3.0W/m.K.	✔	✔	✔	✔
VT-4B5	4.2W/m.K.	✔	✔	✔	✔
VT-4B7	6.5W/m.K.	✔	✔	✔	✔

VIEW THERMAL MANAGEMENT PRODUCTS

Wherever technology takes you, we deliver.

Ventec Europe
www.ventec-europe.com

Ventec USA
www.ventec-usa.com

Ventec International Group
www.venteclaminates.com

IPC-2581 Advances

I am a strong advocate of the IPC-2581B unified file format, because it will simplify the transfer of PCB designs from CAD tools to board manufacturers, incorporate rich attributes that help thoroughly explain exactly what designers intend manufacturers to build, and ease stackup development. The standard aggregates all the elements of a design, every aspect from the stackup to assembly operations, in a single common format for transmission from the CAD platform to the manufacturer.

In my November 2013 column in The PCB Design Magazine, I described what my company experienced as the manufacturer of a test vehicle, a 12-layer network line card designed by Fujitsu Network Communications, which was sent to us as an IPC-2581A file (version A preceded the current version of the standard). We traced some minor anomalies to evaluation software supplied by our CAM vendor, which I understand have been corrected, but we proved the integrity of the IPC-2581A design file. Under the auspices of the IPC-2581 Consortium, which now numbers 60 member companies (see www.ipc2581.com), there have since been major enhancements to the standard and there is work underway to explore how it could integrate other elements to augment conventional PCB description and manufacture, such as device firmware.

The most significant new provision in the B version, from my vantage point as a manufacturer, is the ability to develop a stackup interactively with a designer. Gary Carter, one of the consortium founders and senior manager for CAD engineering at Fujitsu Network Communications, put this in perspective during a recent conversation.

"Material stackup is now supported in RevB. That's a big win in the early part of design, when designers spend a lot of time talking with their fabricator about the choice of materials to meet the design requirements they specified," Carter explained. "Today, it's the passing of napkins, telephone calls, and maybe at the end of the day a JPEG or PDF file from the fabricator following the dialog. Then they [the designers] have to hand-enter the particulars back into their CAD system."

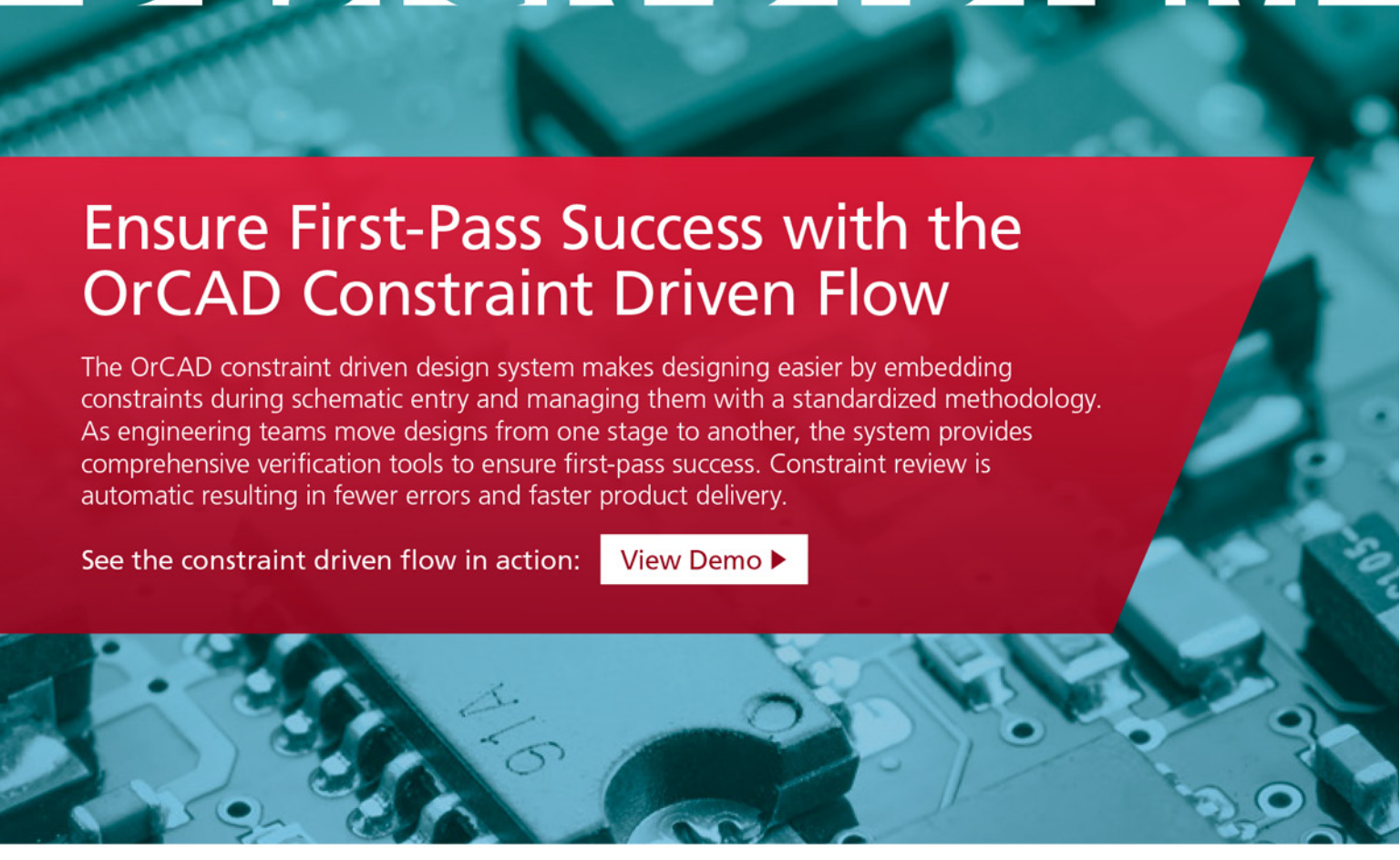
> ***"Material stackup is now supported in RevB. That's a big win in the early part of design, when designers spend a lot of time talking with their fabricator about the choice of materials to meet the design requirements they specified."***

Carter continued, "With RevB, we've demonstrated the capability to move information from a CAD system into a SI tool that has some knowledge of materials and from there, back over to a fabricator, who can respond with suggestions. We can then go back into the same tool and verify that the attributes of the suggested materials do in fact yield the correct results, and then [seamlessly] go back into the CAD system to finalize the stackup, and off we go."

There is no paper involved, and the bidirectional exchanges between the designer and the manufacturer during the stackup development take place via the CAD tool that will render the design. The ability to develop and communicate design information in a consistent format in the same electronic medium from the very inception of a project at the stackup stage all the way through to the CAM equipment used for production ensures that no detail will be misplaced or misinterpreted. This is indeed a big win. **PCBDESIGN**

Amit Bahl directs sales and marketing at Sierra Circuits, a PCB manufacturer in Sunnyvale, California. He can be reached by clicking here.

THE ERROR PREVENTION RESULTS OPTIMIZATION FASTER TO MARKET STAY FRIENDS WITH YOUR COWORKERS DESIGN SYSTEM



Ensure First-Pass Success with the OrCAD Constraint Driven Flow

The OrCAD constraint driven design system makes designing easier by embedding constraints during schematic entry and managing them with a standardized methodology. As engineering teams move designs from one stage to another, the system provides comprehensive verification tools to ensure first-pass success. Constraint review is automatic resulting in fewer errors and faster product delivery.

See the constraint driven flow in action: View Demo ▶

OrCAD™
CADENCE PCB SOLUTIONS

EMA Design Automation®

A PCB Potpourri

by Bob Tarzwell with Dan Beaulieu

Every Process Can be Improved

Dan Beaulieu: I brought Bob Tarzwell into Rockwell Collins' Cedar Rapids office to help with the company's technology. On Bob's first day there, after he'd told them about being hit by lighting twice in one day, Plant Director Mike Driscoll asked Bob if he wanted to take a tour of the facility.

Without batting an eye, Bob said, "Listen, Mike, I'll not only go on a tour with you, but I can promise you that by the end of the tour, I will give you a list of things that you can do immediately that will save you at least $250,000 a year."

Now he really had everyone's attention. These were the guys who were responsible for running the shop as cost-effectively as possible. In fact, Bob was telling them that they were not doing their job right and he could prove it.

Mike just put his head back and roared. Then he said, "Really, you think you can do that, huh?"

"I don't *think* I can do that, I guarantee it." Bob said.

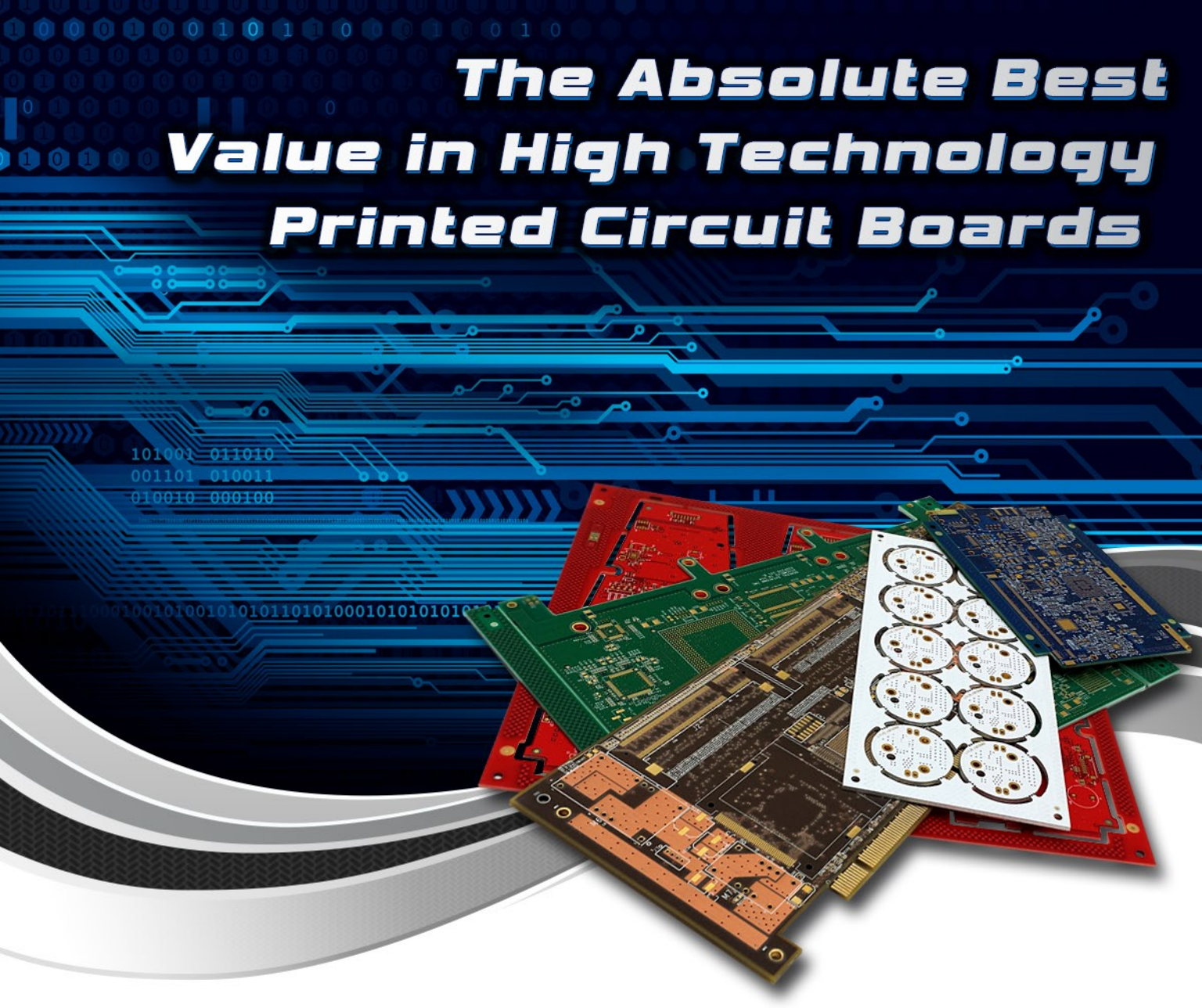
I could sense that Mike was looking at me, but if he was, all he could see was the top of my head because I was holding it in my hands and shaking it. And Bob just kept on going in a way that I thought was closely related to the old saying, "Give a man enough rope…"

Mike said, "You know Bob, I've got to tell you that now you have my full attention. You say that you can do that right now, today?"

"Sure, but before I do, I need to ask you something."

"Okay," Mike said tentatively, "Go ahead and ask me."

The Absolute Best Value in High Technology Printed Circuit Boards



Since 1979, Eagle Electronics Inc. has provided our Customers with the highest quality Printed Circuit Boards at fair and competitive prices. We are committed to exceeding our Customers' expectations and requirements, acheiving **total customer satisfaction** on each and every job. It's just the way we do business!

With Eagle, you can expect:

- Rapid Response to Quote Requests
- Fair and Competitive Pricing/Costs
- 100% Quality Performance
- 100% On-Time Delivery Performance
- Flexibility Scheduling
- Stock/Consigned Inventory Programs
- Thorough follow-up after job completion
- Total Satisfaction!

EAGLE electronics Inc.

MANUFACTURERS OF QUALITY PRINTED CIRCUIT BOARDS

click here for a virtual tour of our facility!

www.eagle-elec.com

A PCB POTPOURRI *continues*

"Are you going to hire me to bring heavy copper into this place?"

Mike laughed again and said, "Of course I'm going to hire you; why do you think we flew you all the way out here today, for the hell of it? Why do you think you're here?"

Bob smiled and said, "All right then, I'm ready for that tour now."

And off they went, trailed by all of those engineers ready to see what this lunatic had to say about their shop. I had seen the shop and number of times, so I decided to pass on the tour. The last I saw of them, Bob was waving his arms and talking a mile a minute while Mike kept laughing and his boys took copious notes.

They were together for four hours on that tour, and judging from the way they got along that night at the steakhouse, I would say that it was time well spent.

Six months later, I was sitting in Mike's office. We were going over the project and talking about how we could best move forward when I remembered Bob's challenge to Mike.

"Remember when Bob came here that first day and you were about to take him on a plant tour?" I asked. "And he told you that he could save you a quarter million dollars while he walked through the plant."

"Yeah?" Mike replied. This time a grin spread across his face.

"Well, how did that turn out? Did he in fact save you all of that money? Did you save $250,000 by using his suggestions?"

"No we didn't get $250,000 in savings."

"Really? That didn't work, huh?"

"No I didn't say that. I said that we didn't get $250,000 in savings, because what we did get was $500,000 in savings," said Mike. "He found a ton of things that we could save money on and I had them all implemented right away. That guy was worth a lot of money to us. You gave us a pretty good deal with that guy."

"Every once and a while, you wind up in a situation where you just want to yell, "What are you, stupid?"A few years ago, I was consulting for a high-tech company. The lead engineer was a know-it-all who personified "The Emperor's New Clothes." He had eight engineers under him, all armed with PhDs, all following him around like he was, in fact, the emperor. They nodded their heads no matter what he said."

The Board That Can't be Built

Bob Tarzwell: Every once and a while, you wind up in a situation where you just want to yell, "What are you, stupid?" A few years ago, I was consulting for a high-tech company. The lead engineer was a know-it-all who personified "The Emperor's New Clothes." He had eight engineers under him, all armed with PhDs, all following him around like he was, in fact, the emperor. They nodded their heads no matter what he said.

The story starts with me being called into a meeting. These engineers wanted to make a new PCB for the emperor, and they handed me a fancy piece of paper that showed the design all neatly done in AutoCAD. It certainly looked like a real PCB.

As the engineers were discussing the new design, I checked it out for the first time. The board measured 230 by 230, with nine 25 wide holes in 25 wide pads with 25 wide traces. Now, mind you, none of the so-called professionals had any PCB design or manufacturing experience.

I interrupted by blurting out, "Excuse me, but what scale are you using? Is this 230 mils, inches, millimeters, or furlongs?" The room fell eerily silent, because the lowly consultant PCB expert had dared to question the emperor's men. The look on their faces said it all. Who is he to question the emperor's people who have PhDs?

The emperor's head guard royally stated, "Microns." He shot me a look that said to keep quiet. Now, here's where I got fired. He kept dis-

cussing how they planned to make this PCB, and I actually laughed out loud.

I blurted out, "Microns?" Yes, unfortunately, my mouth was in gear. "Are you guys nuts? You want to make a PCB that's .009" by .009" with nine .001" holes centered in a .001" pad?" I then held up a blank piece of paper and put a pen dot on the center of the page.

"You mean one-tenth as big as this tiny little dot? How do you plan on routing these out?"

The reply was, "With our drill router." I laughed again.

"That old Excellon 2000? The best you can do is 3–4 mils of tolerance half the size of the board. Any idea how you're going to drill a .001" hole in a .001" pad?"

The reply was, "With the same drill."

"News flash! At 160,000 rpm, you are not going to drill a .001" hole, and, oh yeah, you can't buy .001" drill bits anyway."

At an earlier meeting, our emperor had waved his mighty staff and decreed from on high that we were not allowed to use a laser. I continued unabated, "As you're not allowed to use a laser, how are you going to drill the holes? And what about plating and drill tolerances? You need bigger drills and bigger pads."

I got the strange sense that my presence was not appreciated or wanted. Oh well. I did not much like the little emperor or his court of meek yes-men. Time to look for another job!

Why the Focus on Polyimide?

Bob Tarzwell: I consistently do battle in one arena: Polyimide laminates. It seems that anytime a designer wants a tougher board or higher temperature, he demands polyimide and the laminate of choice. Yet I design and make very high-tech, high-voltage printed circuits all the time and I never use polyimide. Why? Because it absorbs moisture at twice the rate of FR-4, and moisture is an enemy of high-reliability circuits. With polyimide, it is also hard to get the prepreg to flow just right when we make multilayer boards, and it leaves micro holes all through the final PCB. Micro holes are also the enemy of high reliability due to trapped moisture, lowering the laminate's voltage ability over time.

Yes, polyimide can take a higher temperature than any other laminate, but the upper temperature limit is not the only qualifying attribute I consider. I need laminates that press out with a minimum of micro holes, flows well, and holds the minimum voltage rating with time and temperature. I like laminates that limit electroless wicking, and polyimide does not do a great job here. I cringe when designers quote glass transition temperature (Tg) as the reason for using a specific laminate. I have not used or worried about Tg for eight years, ever since I discovered the challenge we face each day with PCB and copper thickness in the holes.

When I look for really tough laminates for downhole PCBs or very high-current, high-voltage PCBs, I use Isola 370 HR or Panasonic 1755. I don't look at Tg; I use decomposition temperature (Td), the temperature at which the laminate starts to lose mass. After I addressed the main worry about Tg, which is the higher expansion of the Z-axis, I moved up to Td. When I design higher-voltage PCBs, from 1,000–15,000 volts, I laminate in a flex sheet core with its higher voltage per mil rating. The only time I use polyimide is for burn-in boards where it is all about maximum temperature with time. But, mind you, some of the new laminates the guys have been coming up lately with are great new tools, and I look forward to working with some of them to help with the extreme boards I work with. **PCBDESIGN**

Bob Tarzwell is a PCB consultant who has spent 50 years in the PCB industry, inventing technology and building almost every type of PCB. He is the co-owner of DB Publishing, the publisher of the PCB 101 and Quality 101 handbooks. Visit www.dmrpcb.com.

Dan Beaulieu is a well-known industry consultant and co-owner of DB Publishing. His column *It's Only Common Sense* appears Monday mornings in the I-Connect 007 Daily Newsletter. He can be reached at danbbeaulieu@aol.com.

HDI PWB Reliability

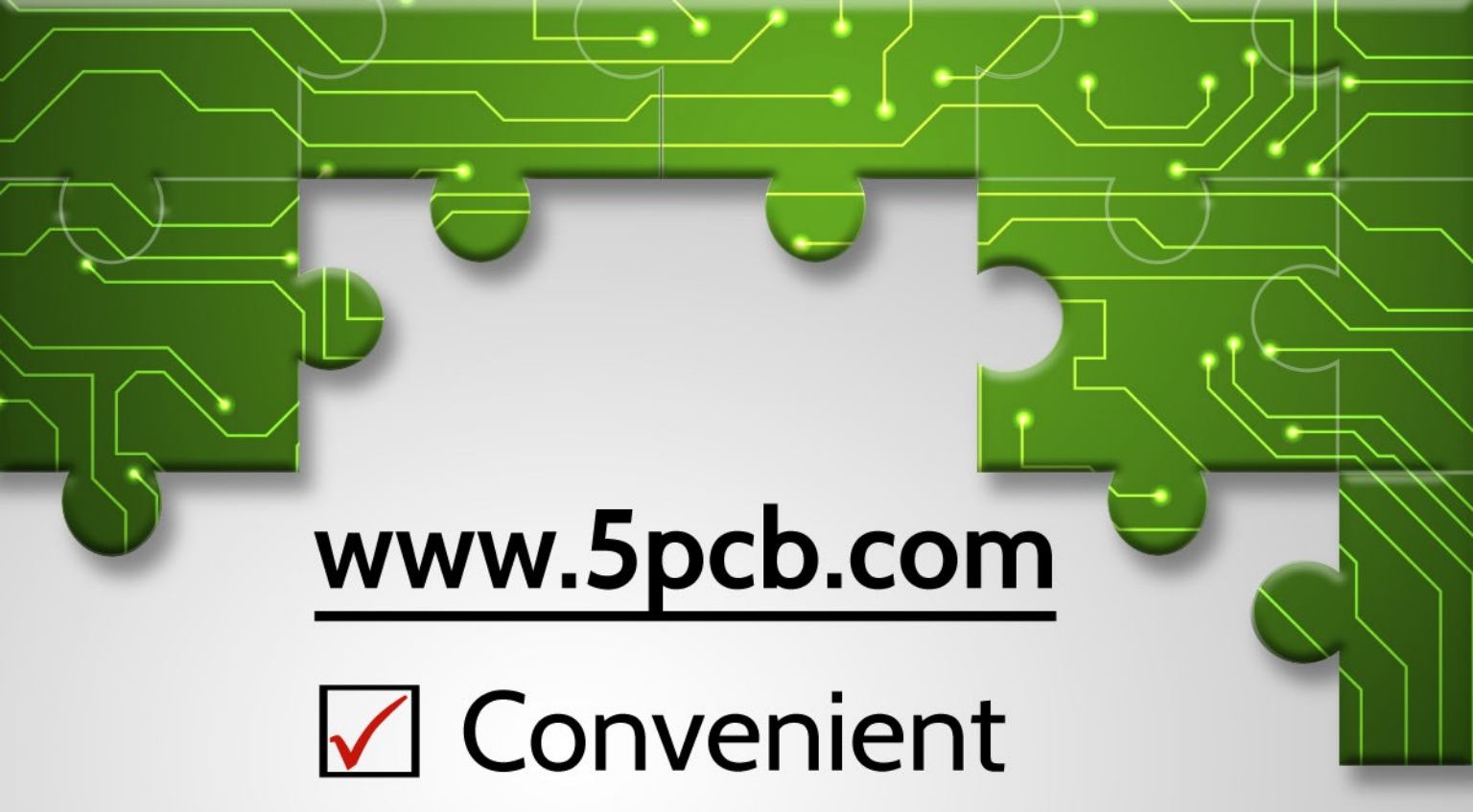
by Paul Reid

An HDI PWB may be defined as a PWB with a higher wiring density per unit area than conventional PWB. They have smaller lines and spaces, smaller vias and capture pads and higher connection pad density than employed in conventional PWB technology. HDI boards utilize microvias, buried vias and sequential lamination with insulation materials and conductor wiring for higher routing density. HDI is an alternative to high layer-count and standard laminate or sequentially laminated boards.

HDI boards are characterized by high-density attributes including laser microvias, fine lines, smaller grid sizes and high performance thin materials. This increased density enables more functionality per unit area. Higher technology HDI PWBs have multiple layers of copper-filled, stacked microvias, which create a structure that enables even more complex interconnections. These very complex structures provide the necessary routing solutions for today's large pin-count chips utilized in mobile devices and other high technology products.

When it comes to HDI reliability, what we must do is consider two parts: the copper interconnects and the base material. What one can do is test the reliability with thermal cycling using Interconnect Stress Test (IST) coupons. The IST coupon tests the copper interconnection and checks for material damage. The coupon is fabricated on the production panel with the PWBs and has all the attributes of the PWB. So the coupon has the same construction, copper weights, hole sizes, grid sizes, and copper plating as is found in the corresponding board. The test thermal cycles the IST coupon, typically for 500 cycles, or until the coupon fails with a 10% increase in resistance due to cracks that develop in copper interconnections as a result of thermal cycling.

By measuring capacitance change between ground planes we can determine if there is any significant material damage in the coupon. One must measure the capacitance in picofarads between adjacent ground planes before testing (to establish a base line), after preconditioning (a simulation of assembly and rework) and at the end of test. We then compare the measurement after preconditioning and at the end of test to



www.5pcb.com

- ☑ Convenient
- ☑ Fast delivery
- ☑ High quality
- ☑ Low prices

With our online system, getting quotes and placing orders is fast, simple and convenient. In fact every step of the process can be managed online–even payment! And our quality is guaranteed.

All you need to get started is to set up your account.

Create free account

DME

D.M. Electronic International Co., Ltd.

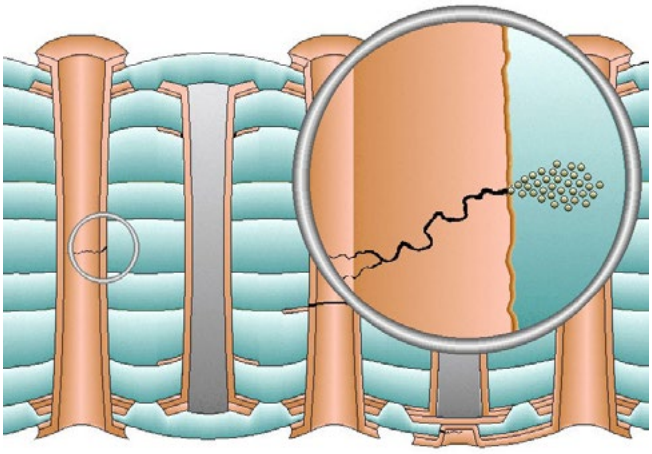


Figure 1: Barrel crack due to metal fatigue.

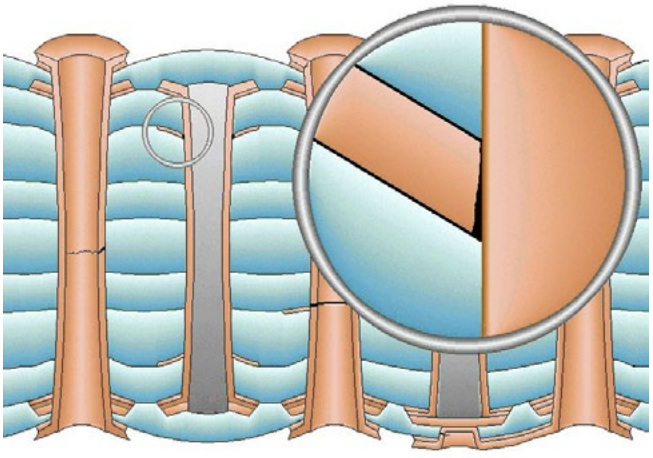


Figure 2: Interconnect separation.

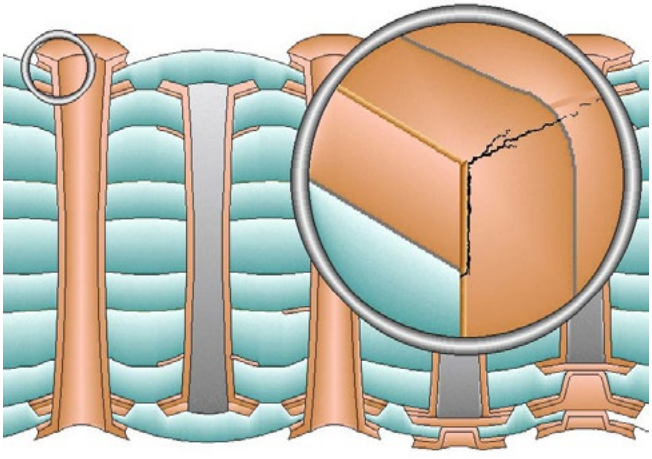


Figure 3: Corner or knee crack.

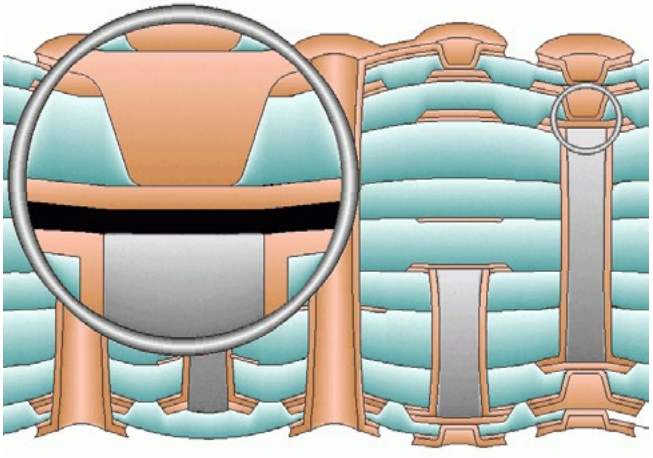


Figure 4: Lifted copper cap on buried via.

those original readings. A -4% change or greater indicates significant material damage and a cross section is processed to confirm or refute this finding.

The major problem is the implementation of lead-free soldering that requires assembly temperatures of 260°C. The FR-4 material is at its limit to withstand the heat when exposed to 260°C. The Z-axis expansion is at its highest at this temperature, putting extra strain on the copper interconnects.

The most common type of failure of a robust interconnection is a barrel crack that occurs in the central zone of the plated through hole (PTH). When tested using thermal cycling to 150°C, this is a wear-out type of failure that happens over hundreds of cycles (500+ cycles). Surviving 500 cycles without any significant increase in resistance is considered a robust coupon.

In a weak coupon, the failure before 350 cycles may relate to a process problem, with the most common problem being thin copper plating. With thin plating, the barrel cracks may still be the cause the failure but it would be failing in less than 350 cycles. The PTH may also fail for corner cracks or interconnection separation.

Weak buried vias fail typically for barrel cracks in the center zone of the structure similar to PTHs and, less often, for corner crack or interconnect separation. One of the HDI structures includes microvias stacked on buried vias.

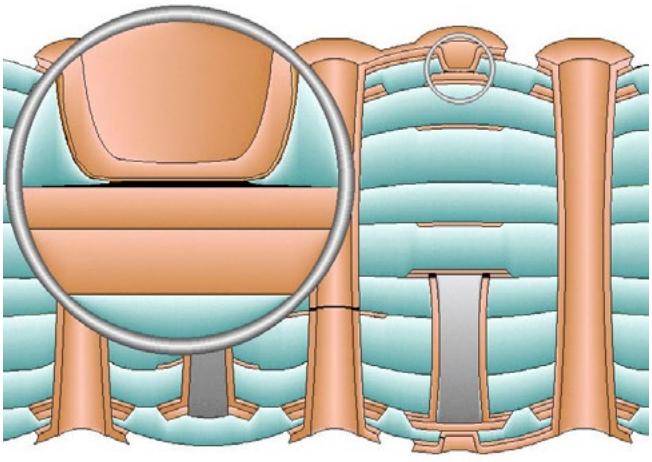


Figure 5: Microvia separation.

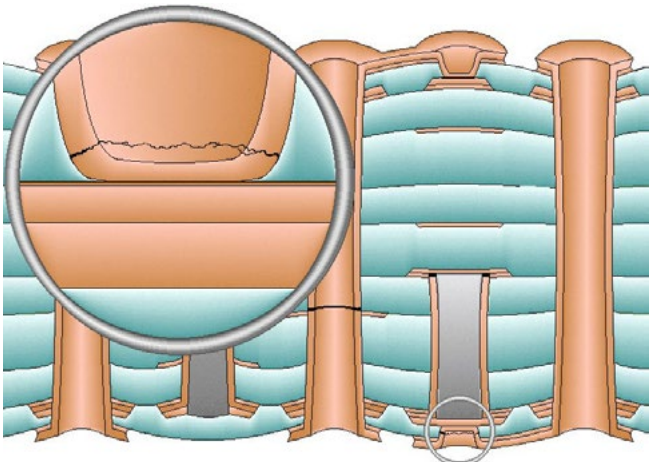


Figure 6: Microvia barrel crack.

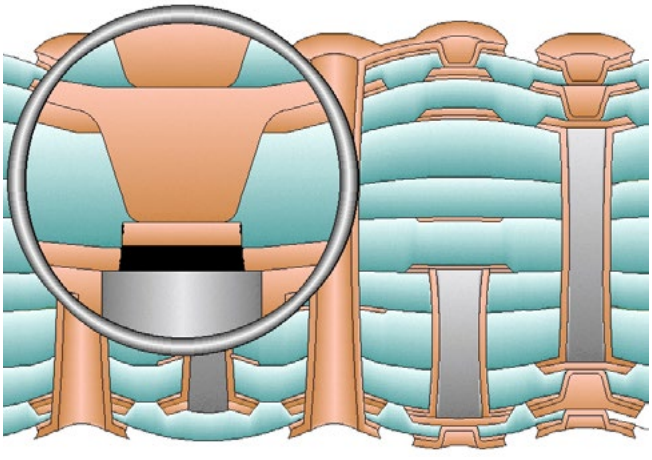


Figure 7: Microvia pull out failure.

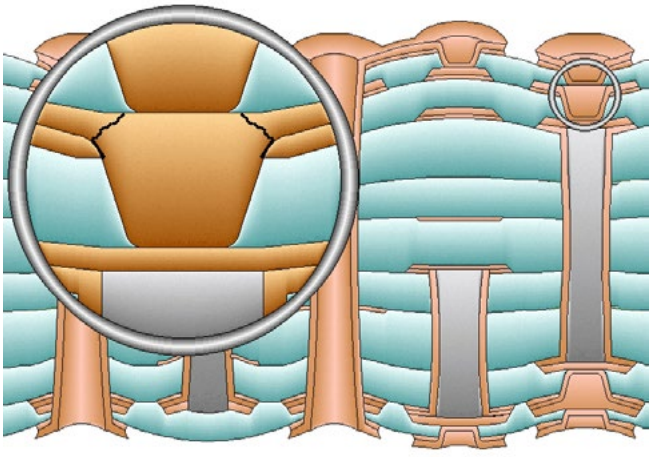


Figure 8: Microvia corner crack.

In order to have a microvia stacked on top of the buried via what we have to have is a conductive cap on the top of the buried via, which can also fail. There may be a separation of the copper cap from the top of the buried via or a crack in the cap of the buried via (Figure 7).

Microvias are typically the most robust type of interconnection. Because of their robustness they are tested at 190°C. When tested at 190°C, robust microvias will survive 500 cycles while weak microvias will fail before 500 cycles. The most common cause of microvia failure is a separation between the base of the microvia and the target pad. The second most common cause of microvia failure is a barrel crack toward the base of the microvia. Other failure modes include corner cracks (seen in copper-filled microvias) and pull out types of failures where the target pad cracks around the base of the microvia.

In HDI PWBs one must also consider construction. One may produce multiple microvias structures as either stacked or staggered. Microvias that are stacked are about four times more vulnerable to failure than the same structure in which the microvias are staggered. Well fabricated one- and two-layer microvias do not usually fail prematurely. Three- and four-stacked microvias tend to fail before 500 cycles when tested at 190°C and are a fabrication challenge.

The material damage is monitored in an IST coupon by measuring changes in capacitance

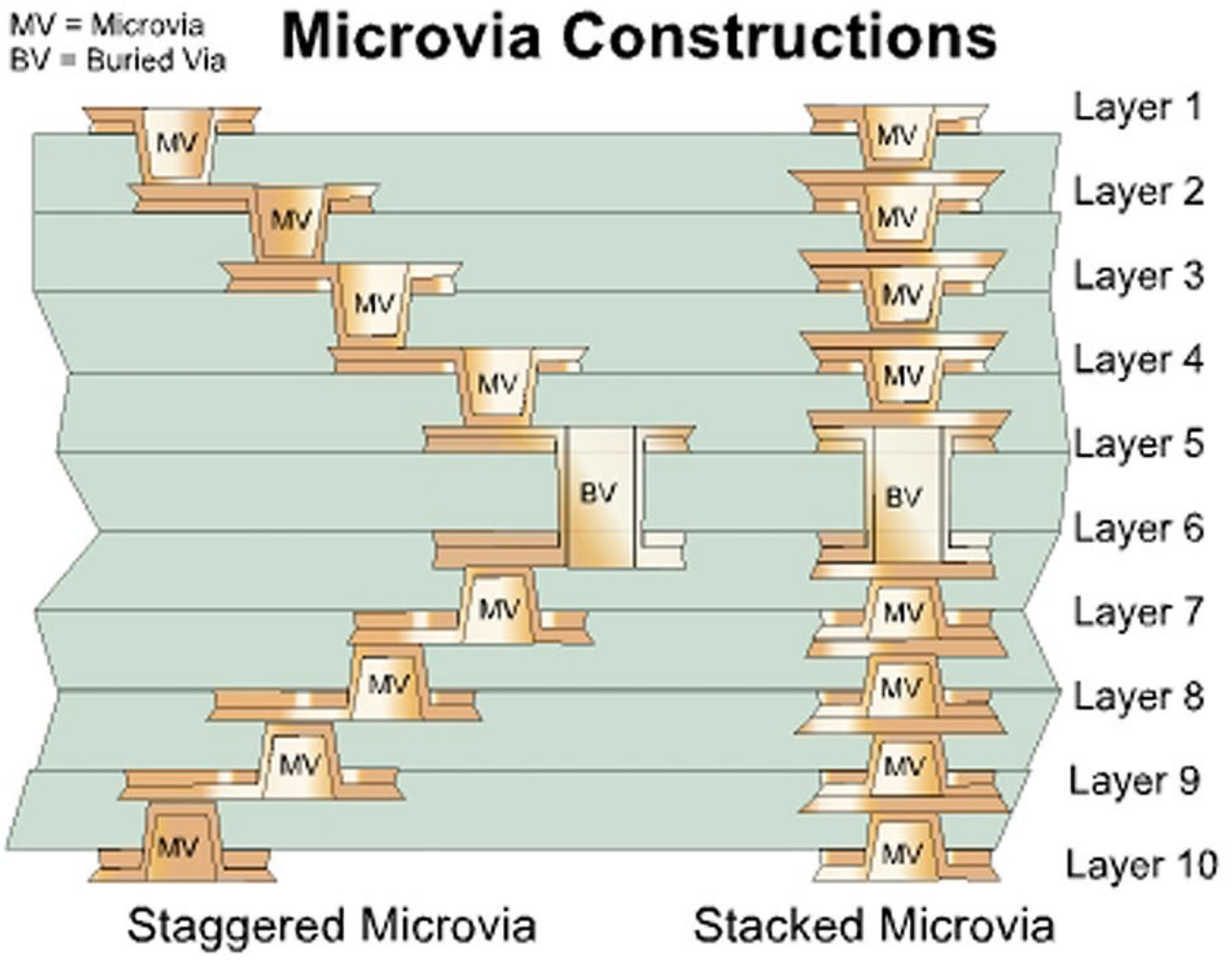


Figure 9: Staggered vs. stacked microvias.

between ground layers in the coupon. First, measure the capacitance between two flooded ground planes in the coupons in the as-received state and then again after the coupon has undergone preconditioning, and at the end of test. If there is significant material damage then a -4% or greater drop in capacitance is seen. To confirm the drop in capacitance is indicative of material damage, one or two of the coupons are subjected to a microsection to check for the presence of material damage.

The major types of material damage found are adhesive delamination, cohesive cracks, and crazing. Adhesive delamination is typically between two laminated surfaces like the b-stage, c-stage and copper interfaces. On occasion, adhesive delamination is seen between the glass bundles as a group and epoxy of the dielectric. This type of failure is found typically on a 1 mm (.040″) grid or greater.

The most common type of material damage is the cohesive crack, which is a crack that goes through the b-stage, c-stage and glass bundles. The cohesive failure is a breakdown of the epoxy system due to high temperatures of assembly. This type of failure is found typically on a 0.8 mm (.032″) grid.

Crazing is the separation between glass fibers and the epoxy system. It looks like silver sheen on the glass bundles due to an envelope of air around the glass fiber. Crazing provides a pathway for conductive anodic filament (CAF) formation. This type of failure is found typically on a 0.5 mm (.020″) grid.

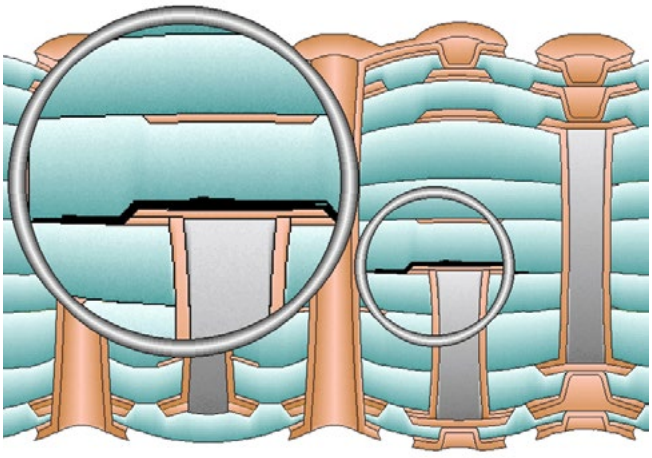


Figure 10: Adhesive delamination.

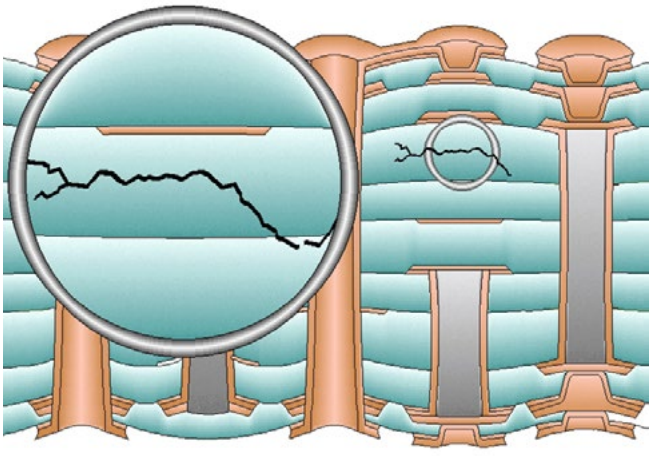


Figure 11: Cohesive crack.

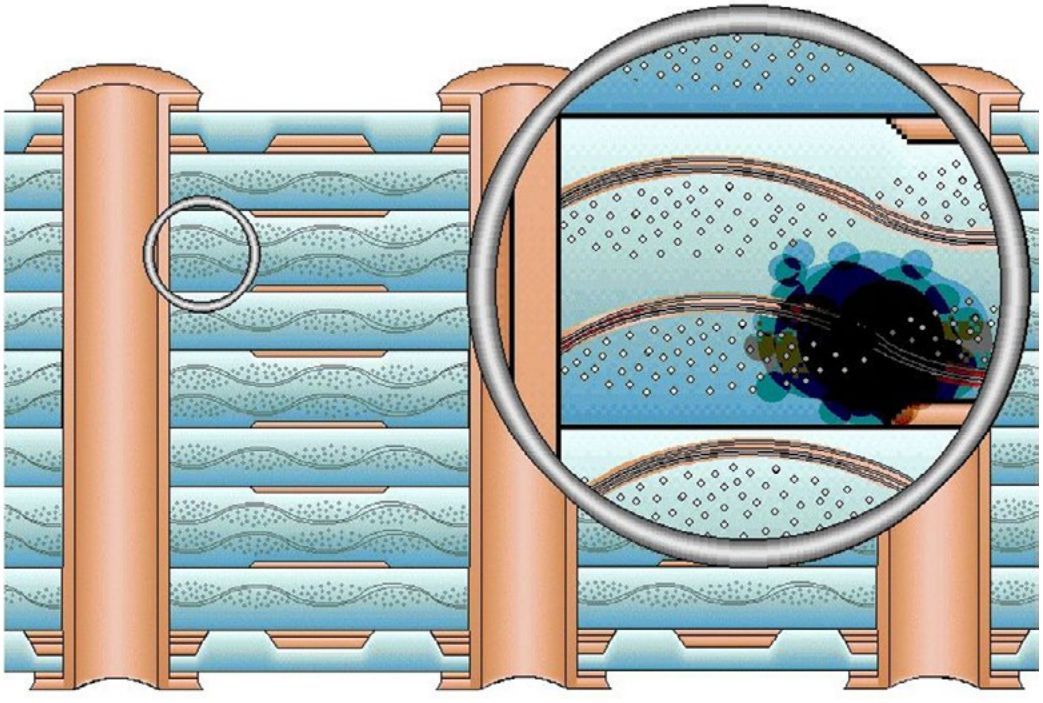


Figure 12: Crazing with a CAF failure.

In conclusion, the use of HDI PWB reliability in lead-free applications is a dual-edged sword. The copper interconnections are more prone to a breakdown and the material is more prone to damage. That is not to say that robust PWBs cannot be made, but there is a challenge in producing them. One must test the interconnect and the material in order to confirm robustness in a given application.

PCBDESIGN

Paul Reid's career in PCB fabrication and reliability testing spans 35 years. One of his specialties is producing technical animations of failure modes induced by thermal excursions, giving him insight into the mechanisms of circuit board failure. Reid is now retired. To contact the author, click here.

Mil/Aero007 News Highlights

Mass Design Earns DLA MIL PRF 55110 Certification

Mass Design Inc. has been awarded the Defense Logistics Agency (DLA) MIL PRF 55110 Certification, establishing this U.S.-based company as a key manufacturer of rigid, flexible, and rigid/flex PCBs for the U.S. Department of Defense.

IPC Responds to DoD on Flex Hybrid & Packaging Tech

In an effort to accelerate development and adoption of cutting-edge manufacturing technologies for making new, globally competitive products with commercial and defense applications, the Department of Defense (DoD) issued a Request for Information (RFI) on future advanced manufacturing centers called Institutes for Manufacturing Innovation, or IMIs.

FTG's Aerospace Segments Show Dramatic Q2 Improvements

"FTG's momentum has continued through the first half of 2014 with strong results across the company, particularly at our two new aerospace facilities in Tianjin and Chatsworth where we continued to see progress on qualification activities, strong orders, and increased shipments," stated Brad Bourne, president and CEO.

IPC PERM Council Addresses Lead-free Concerns

The IPC Pb-free Electronics Risk Management Council is currently meeting in Toronto, to discuss lead-free conversion issues related to the safety, performance, and reliability of electronics in the aerospace, defense, medical, and other high-performance markets. The Council develops and coordinates risk management approaches for the transition to lead-free electronics.

ACI Names Circuit Solutions Mid-Atlantic Region Rep

Bryan Ricke, director of sales and business development, stated, "We are excited to partner with Circuit Solutions LLC, led by the team of John Vaughan and Jesse Vaughan, to promote our broad and unique product offering geared to the RF community. Their outstanding reputation in the electronics industry coupled with a smart, solutions-driven and vertically integrated business model is a win-win strategy for all parties."

Dragon Circuits Achieves MIL-P-50884E Recertification

The recertification will allow Dragon to continue the manufacture of PCBs with adhesive/adhesiveless base for critical military-based applications.

Multilayer Completes MIL-PRF-55110 Recertification

Multilayer Technology is pleased to announce the completion of an additional successful recertification. This current recertification is in addition to the recent Aerospace Supplier (AS9100C) re-certification.

Former Astronaut Helps Murrietta Celebrate Award

When Murrietta Circuits received their Five Star Supplier award from Raytheon in Massachusetts last June, former astronaut and now vice president of Mission Assurance, Quality, and Raytheon's Six Sigma for Integrated Defense Systems (IDS), Robert Curbeam, handed them the award.

Canadian Circuits Nets Controlled Goods Certification

Praveen Arya, president and co-owner of Canadian Circuits, Inc. announced that his company has received its Canadian Controlled Goods Certification. This, along with their ITAR Registration, makes the company a viable PCB source for all military and aerospace companies requiring these certifications.

DARPA Details Next-Gen GPS Technologies

Several new programs are exploring innovative technologies and approaches that could eventually provide reliable, highly-accurate positioning, navigation, and timing capabilities when GPS capabilities are degraded or unavailable. Penny-sized inertial sensors, pulsed lasers, and tracked lightning strikes are among the novel approaches to provide location-based insights in GPS-denied areas.

" Providing *Solutions* to Board Fabrication Challenges"

FROM CONCEPT TO COMPLETION

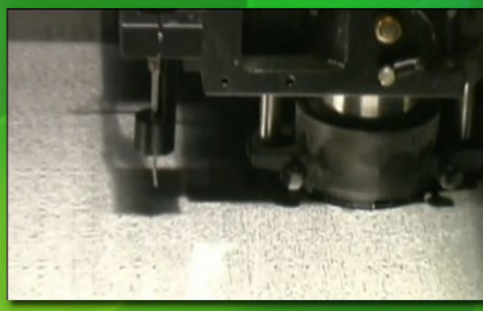
Solutions for Every Complex Situation

At Multilayer Technology we have the skills and the knowledge to be able to say "Yes We Can!" to your most complex design requirements.

We specialize in High-Speed Digital and RF Design constraints. In addition, we offer the following solution-based services:

- Extensive Exotic Material Processing
- Pre-DFM Services Available
- State-of-the-Art Industry Leading Processes
- Space-Based Reliability Requirements Standard

REQUEST A QUOTE



Multilayer Technology
3835 Conflans Rd
Irving, TX 75061-3914

(972) 790-0062

WWW.MULTILAYER.COM

ITAR

Mil-PRF-55110

AS 9100

i-connect007 panel discussion video

The Great File Format Transfer Debate

Sponsored by Gardien Group

Altium's Ben Jordan moderates a multi-perspective look into file format transfer options with panelists Karel Tavernier (Ucamco), Dave Wiens (Mentor Graphics) and Hemant Shah (Cadence).

realtimewith.com

Scientists Develop Thinnest-Possible Semiconductor

Scientists have developed what they believe is the thinnest-possible semiconductor, a new class of nanoscale materials made in sheets only three atoms thick.

The University of Washington researchers have demonstrated that two of these single-layer semiconductor materials can be connected in an atomically seamless fashion known as a heterojunction. This result could be the basis for next-generation flexible and transparent computing, better light-emitting diodes, or LEDs, and solar technologies.

The researchers discovered that two flat semiconductor materials can be connected edge-to-edge with crystalline perfection. They worked with two single-layer, or monolayer, materials--molybdenum diselenide and tungsten diselenide--that have very similar structures, which was key to creating the composite two-dimensional semiconductor.

Collaborators from the electron microscopy center at the University of Warwick in England found that all the atoms in both materials formed a single honeycomb lattice structure, without any distortions or discontinuities. First, they inserted a powder mixture of the two materials into a chamber heated to 900 degrees Celsius (1,652 F). Hydrogen gas was then passed through the chamber and the evaporated atoms from one of the materials were carried toward a cooler region of the tube and deposited as single-layer crystals in the shape of triangles.

After a while, evaporated atoms from the second material then attached to the edges of the triangle to create a seamless semiconducting heterojunction.

Researchers have already demonstrated that the junction interacts with light much more strongly than the rest of the monolayer.

PCB BUYERS - compare nearly 1900 manufacturers now at *The* PCB List.

Quick Search

Advanced Search

thepcblist

The best way to find a PCB fabricator, *anywhere*.

www.thepcblist.com

News Highlights from PCBDesign007 this Month

① Mentor's Solid Q2 Results Driven by Auto Sector

"The second quarter was strong for Mentor and we exceeded non-GAAP earnings guidance," said Gregory K. Hinckley, president. "A four percent revenue upside to guidance, along with continued attention to expense control, drove an over 50 percent beat in earnings per share. Automotive had an exceptional quarter, with record quarterly bookings three times the level of last year."

② Sunstone Announces PCB123 Version 5.1.0

"PCB123's addition of drag-and-drop for parts and the change in uniformity between control panels for layout and schematic views, will have a very big impact on the user's ability to save time and money while designing their PCB," said CAD/EDA Marketing Manager Nolan Johnson.

③ Polar Unveils CITS at PCB West

The company will preview its next-generation CITS880s Controlled Impedance Test System at PCB West 2014, September 10, in Santa Clara, California. The system introduces Launch Point Extrapolation, enabling PCB fabricators to improve impedance control for the latest high-speed PCBs which use finer trace widths and thinner copper compared to conventional boards.

④ Packaging Machinery Supplier Selects Zuken's E3.series

The E3.series will be implemented as part of a strategic initiative to establish an integrated mechatronic product development solution comprising mechanical, controls design, and software engineering. The solution will be implemented over several phases using Zuken's certified project management methodology to ensure achievement of the project scope in a planned and controlled approach.

5 Intercept Strengthens Canadian Representation with Kaltron

"Kaltron is delighted to offer Intercept's PCB, Hybrid IC, and RF software solutions to our customers in Canada. They complement very well our existing portfolio of design services, components, and modules," said Tom Martin, president of Kaltron.

6 dalTools: New Commands at Three Venues in September

The company, a Cadence Connections partner, has announced two new commands recently added to the existing list of 80+ Skill commands in dalTools: dal Enhanced Back Drill and dxf2mcm. dalTools will exhibit these tools at three upcoming September events in the U.S.

7 Intercept Expands in China with EDATC

Intercept Technology Inc. announces its newest authorized reseller, Shenzhen EDA Technologies Co., Ltd. (EDATC). With over 12 years of experience selling and marketing EDA software, Shenzhen EDA Technologies joins the Intercept team in its continued efforts to bring more streamlined, global solutions to the Chinese market place.

8 Mentor Graphics Launches 25th Annual PCB TLA Program

The company has announced the call-for-entries of its 25th annual Technology Leadership Awards (TLA) competition, continuing its tradition of recognizing excellence in PCB design. Started in 1988, this program is the longest running competition of its kind in the EDA industry.

9 Zuken, SiSoft: Multi-gigabit Design & Analysis Solutions

By integrating SiSoft's advanced signal integrity solutions for state-of-the-art, high-speed digital system design with Zuken's 3D multi-board, system-level platform, the two companies will provide a combined design and verification flow. The companies will initially focus on integration between Zuken's CR-8000 tool suite and SiSoft's Quantum Channel Designer and Quantum-SI tools.

10 ANSYS Posts Q2 Revenue Increase

ANSYS has announced results for the second quarter of 2014. The company reported total GAAP revenue of $232.4 million for Q2 2014, up from $214.9 million for the same period in 2013.

events

For the IPC Calendar of Events, click here.

For the SMTA Calendar of Events, click here.

For a complete listing, check out *The PCB Design Magazine's* event calendar.

IMTS 2014
September 8–13, 2014
Chicago, Illinois, USA

PCB Design Conference West
September 9–11, 2014
Santa Clara, California, USA

Hybrid & Electric Vehicles Forum 2014
September 17–18, 2014
Munich, Germany

Medical Electronics Symposium 2014
September 18–19, 2014
Portland, Oregon, USA

FUTURA
September 18–21, 2014
Salzburg, Austria

MEDIX Osaka
September 24–26, 2014
Osaka, Japan

SMTA International 2014
September 28–October 2, 2014
Rosemont, Illinois, USA

Standards Development Meetings
September 28–October 2, 2014
Rosemont, Illinois, USA

CEA Innovate!
September 30–October 2, 2014
Litchfield Park, Arizona, USA

World Energy Engineering Congress (WEEC)
October 1–3, 2014
Washington, DC, USA

NEPCON Vietnam 2014
October 9–11, 2014
Ho Chi Minh, Vietnam

Austin CTEA Expo & Tech Forum
October 14, 2014
Austin, Texas, USA

Long Island SMTA Expo and Technical Forum
October 15, 2014
Islandia, New York, USA

Connecticut Expo & Tech Forum
October 21, 2014
Waterbury, Connecticut, USA

Intermountain (Utah) Expo & Tech Forum
October 23, 2014
Salt Lake City, Utah, USA

Industrial Automation Conference 2014
October 23–24, 2014
London, UK

PUBLISHER: **BARRY MATTIES**
barry@iconnect007.com

PUBLISHER: **RAY RASMUSSEN**
(916) 337-4402; ray@iconnect007.com

SALES MANAGER: **BARB HOCKADAY**
(916) 608-0660; barb@iconnect007.com

MARKETING SERVICES: **TOBEY MARSICOVETERE**
(916) 266-9160; tobey@iconnect007.com

EDITORIAL:
GROUP EDITORIAL DIRECTOR: **RAY RASMUSSEN**
(916) 337-4402; ray@iconnect007.com

MANAGING EDITOR: **ANDY SHAUGHNESSY**
(404) 806-0508; andy@iconnect007.com

TECHNICAL EDITOR: **PETE STARKEY**
+44 (0) 1455 293333; pete@iconnect007.com

MAGAZINE PRODUCTION CREW:
PRODUCTION MANAGER: **MIKE RADOGNA**
mike@iconnect007.com

MAGAZINE LAYOUT: **RON MEOGROSSI**

AD DESIGN: **SHELLY STEIN, MIKE RADOGNA**

INNOVATIVE TECHNOLOGY: **BRYSON MATTIES**

COVER ART: **SHELLY STEIN**

THE pcb design MAGAZINE

September 2014, Volume 3, Number 9 • The PCB Design Magazine© is published monthly, by BR Publishing, Inc.

ADVERTISER INDEX

Coming Soon to *The PCB Design Magazine:*

October:
Signal Integrity

November:
Outsourcing Designs: When Does it Make Sense?

December:
HDI